FIG. 1

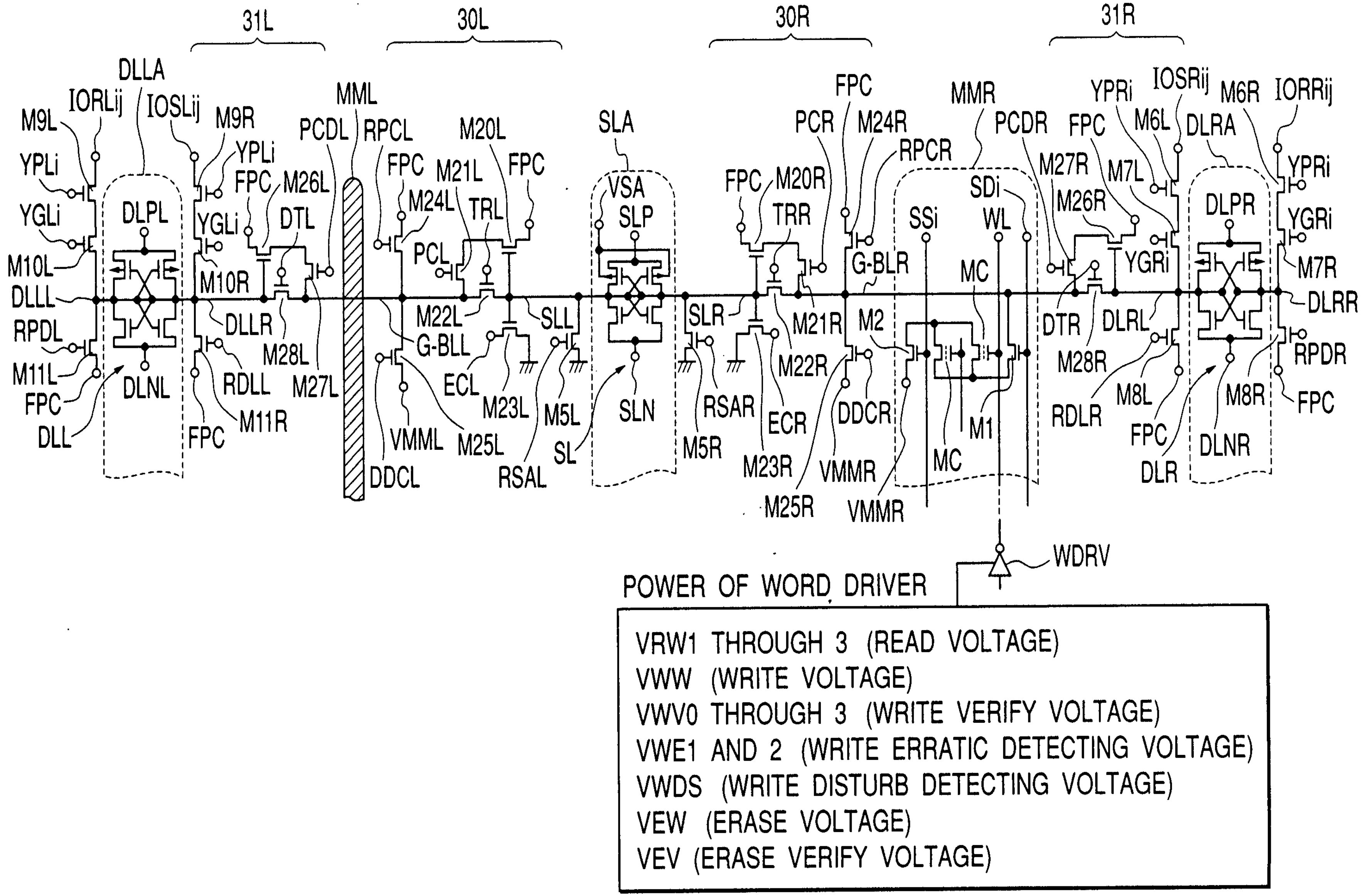

31L
30L
30R
31R
DLLA
M9L
IORLij
IOSLij
M9R
YPLi
YGLi
M10L
DLLL
RPDL
M11L
FPC
DLL
DLPL
DLNL
YPLi
YGLi
FPC
M26L
DTL
M10R
DLLR
M28L
RDLL
M27L
FPC
M11R
MML
PCDL
RPCL
FPC
M24L
PCL
M21L
TRL
M20L
FPC
M22L
G-BLL
ECL
M23L
VMML
M25L
DDCL
SLL
M5L
RSAL
SLA
VSA
SLP
SLN
SL
SLR
M5R
RSAR
FPC
M20R
TRR
PCR
M21R
M22R
ECR
M23R
M25R
FPC
M24R
RPCR
G-BLR
M2
DDCR
VMMR
VMMR
MMR
SSi
SDi
WL
MC
MC
M1
PCDR
M27R
M26R
FPC
YPRi
M7L
YGRi
DTR
DLRL
M28R
RDLR
M8L
FPC
DLR
IOSRij
M6L
DLRA
DLPR
DLNR
M6R
IORRij
YPRi
YGRi
M7R
DLRR
RPDR
M8R
FPC
WDRV
POWER OF WORD DRIVER
VRW1 THROUGH 3 (READ VOLTAGE)
VWW (WRITE VOLTAGE)
VWV0 THROUGH 3 (WRITE VERIFY VOLTAGE)
VWE1 AND 2 (WRITE ERRATIC DETECTING VOLTAGE)
VWDS (WRITE DISTURB DETECTING VOLTAGE)
VEW (ERASE VOLTAGE)
VEV (ERASE VERIFY VOLTAGE)

FIG. 2

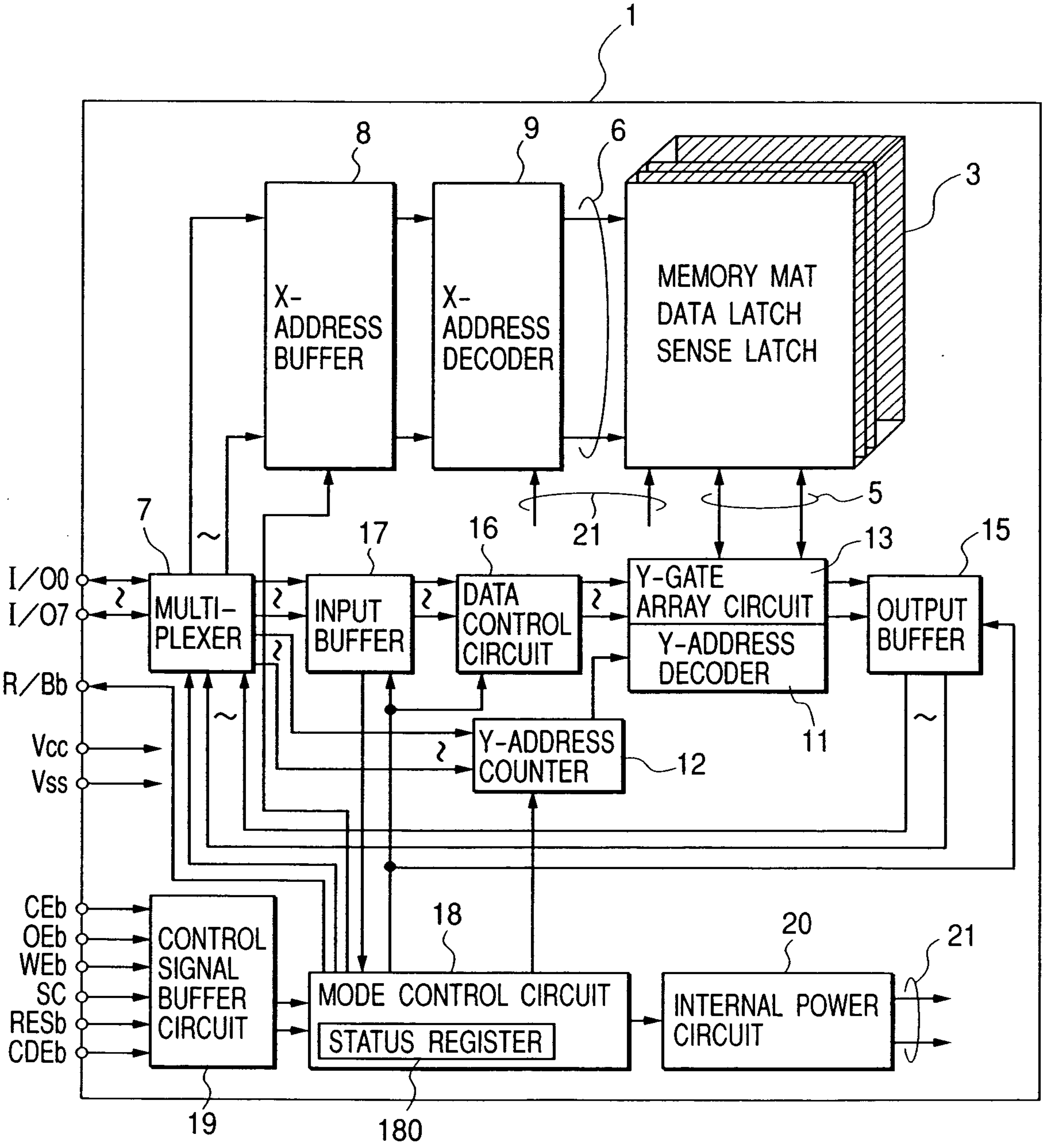

1
8
9
6
3
X-ADDRESS BUFFER
X-ADDRESS DECODER
MEMORY MAT
DATA LATCH
SENSE LATCH
5
21
7
17
16
13
15
I/O0
I/O7
MULTI-PLEXER
INPUT BUFFER
DATA CONTROL CIRCUIT
Y-GATE ARRAY CIRCUIT
Y-ADDRESS DECODER
OUTPUT BUFFER
R/Bb
11
Vcc
Vss
Y-ADDRESS COUNTER
12
CEb
OEb
WEb
SC
RESb
CDEb
CONTROL SIGNAL BUFFER CIRCUIT
18
MODE CONTROL CIRCUIT
STATUS REGISTER
20
INTERNAL POWER CIRCUIT
21
19
180

FIG. 3

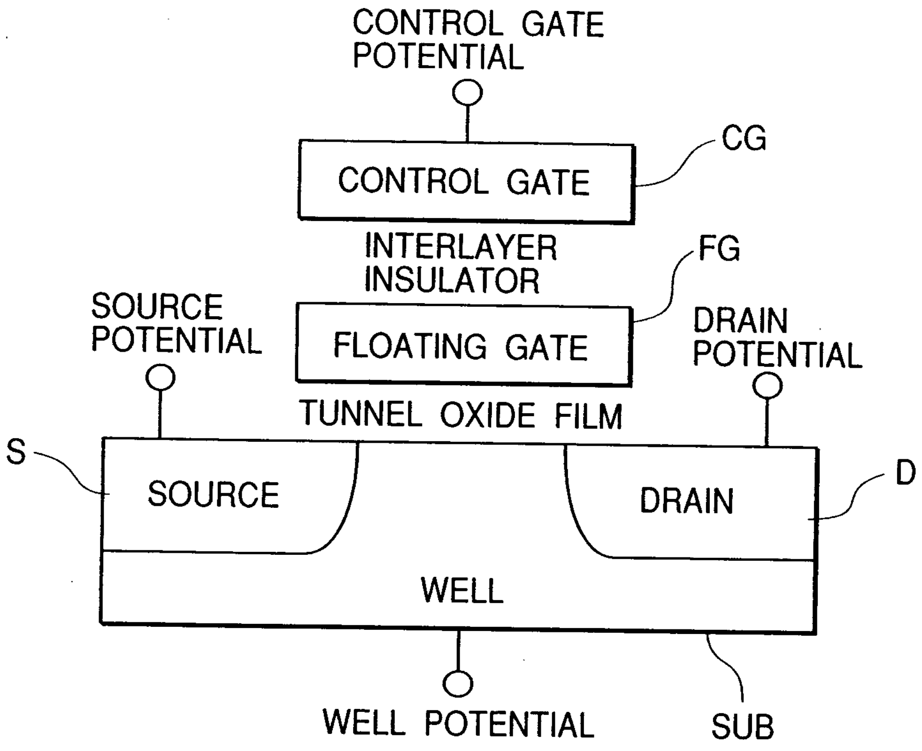


FIG. 4

OPERATING MODE	COMMAND
READ	00H
WRITE	1FH
ADDITIONAL WRITE	10H
ERASE	20H

FIG. 5

	DESIGNATION	DEFINITION
I/O7	Ready/$\overline{\text{Busy}}$	"V_{OH}"=Ready "V_{OL}"=Busy
I/O6	Reserved	
I/O5	Erase Check	"V_{OH}"=Fail "V_{OL}"=Pass
I/O4	Program Check	"V_{OH}"=Fail "V_{OL}"=Pass
I/O3	Reserved	
I/O2	Reserved	
I/O1	Reserved	
I/O0	Reserved	

STATUS REGISTER

FIG. 6

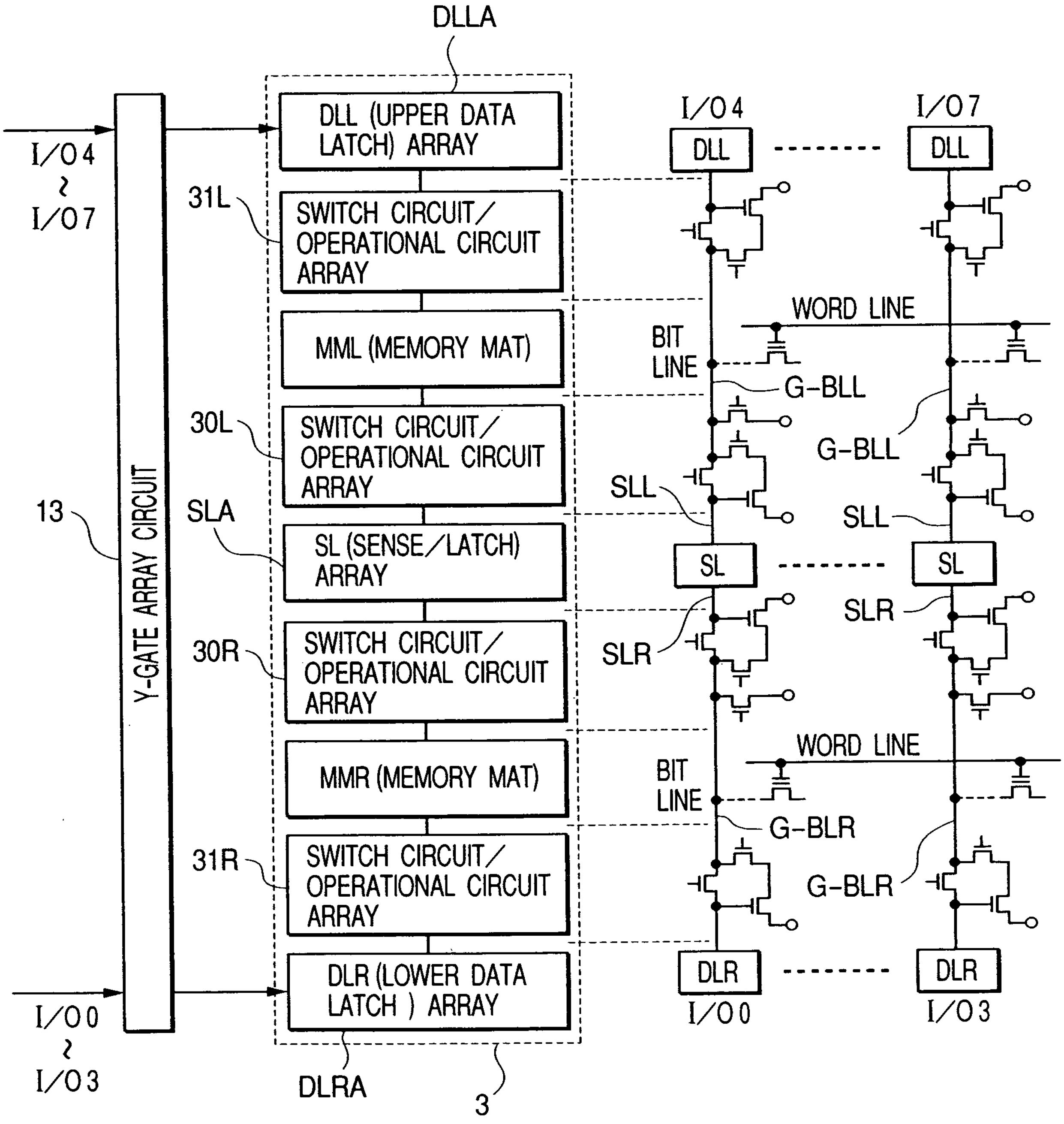

DLLA
I/O4
~
I/O7
Y-GATE ARRAY CIRCUIT
13
DLL (UPPER DATA LATCH) ARRAY
31L
SWITCH CIRCUIT/ OPERATIONAL CIRCUIT ARRAY
MML (MEMORY MAT)
30L
SWITCH CIRCUIT/ OPERATIONAL CIRCUIT ARRAY
SLA
SL (SENSE/LATCH) ARRAY
30R
SWITCH CIRCUIT/ OPERATIONAL CIRCUIT ARRAY
MMR (MEMORY MAT)
31R
SWITCH CIRCUIT/ OPERATIONAL CIRCUIT ARRAY
DLR (LOWER DATA LATCH) ARRAY
DLRA
3
I/O0
~
I/O3
I/O4
I/O7
DLL
DLL
WORD LINE
BIT LINE
G-BLL
G-BLL
SLL
SLL
SL
SL
SLR
SLR
WORD LINE
BIT LINE
G-BLR
G-BLR
DLR
DLR
I/O0
I/O3

FIG. 7

WRITE DATA	I/O		DLL	DLR
	4	0		
01	0	1	0	1
00	0	0	0	0
10	1	0	1	0
11	1	1	1	1

INPUT WRITE DATA

FIG. 8

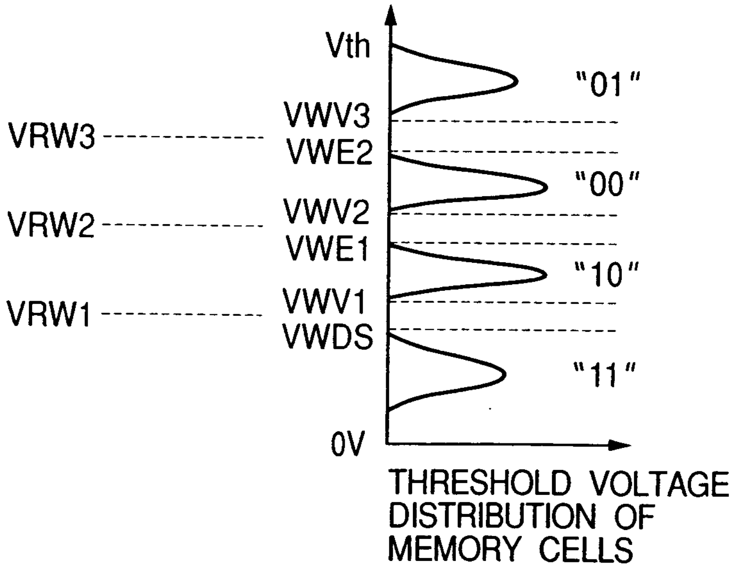


FIG. 9

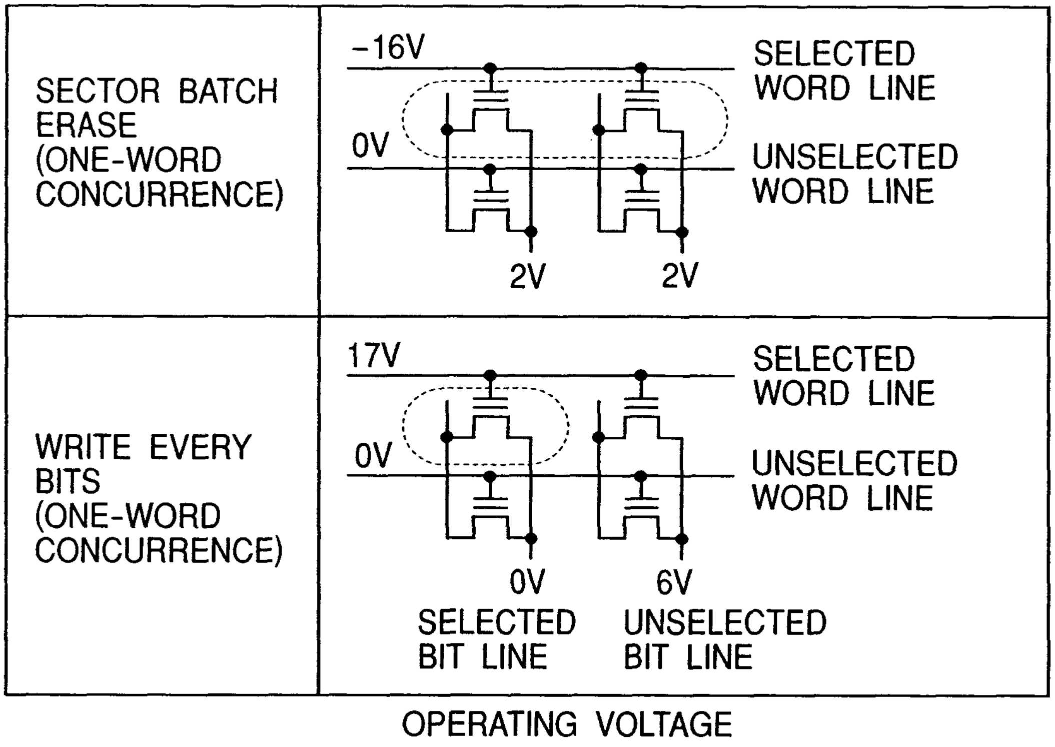

SECTOR BATCH ERASE (ONE-WORD CONCURRENCE)
-16V
SELECTED WORD LINE
0V
UNSELECTED WORD LINE
2V
2V
WRITE EVERY BITS (ONE-WORD CONCURRENCE)
17V
SELECTED WORD LINE
0V
UNSELECTED WORD LINE
0V
6V
SELECTED BIT LINE
UNSELECTED BIT LINE
OPERATING VOLTAGE

FIG. 10

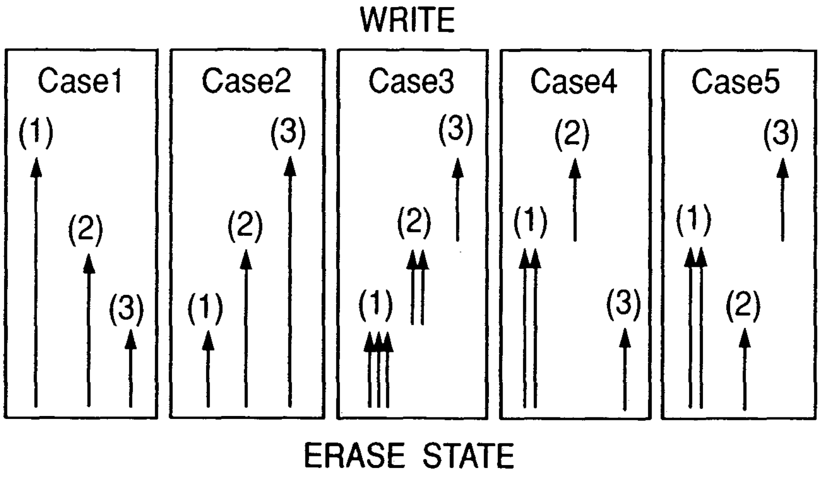

WRITE
Case1
(1)
(2)
(3)
Case2
(3)
(2)
(1)
Case3
(3)
(2)
(1)
Case4
(2)
(1)
(3)
Case5
(3)
(1)
(2)
ERASE STATE

FIG. 11

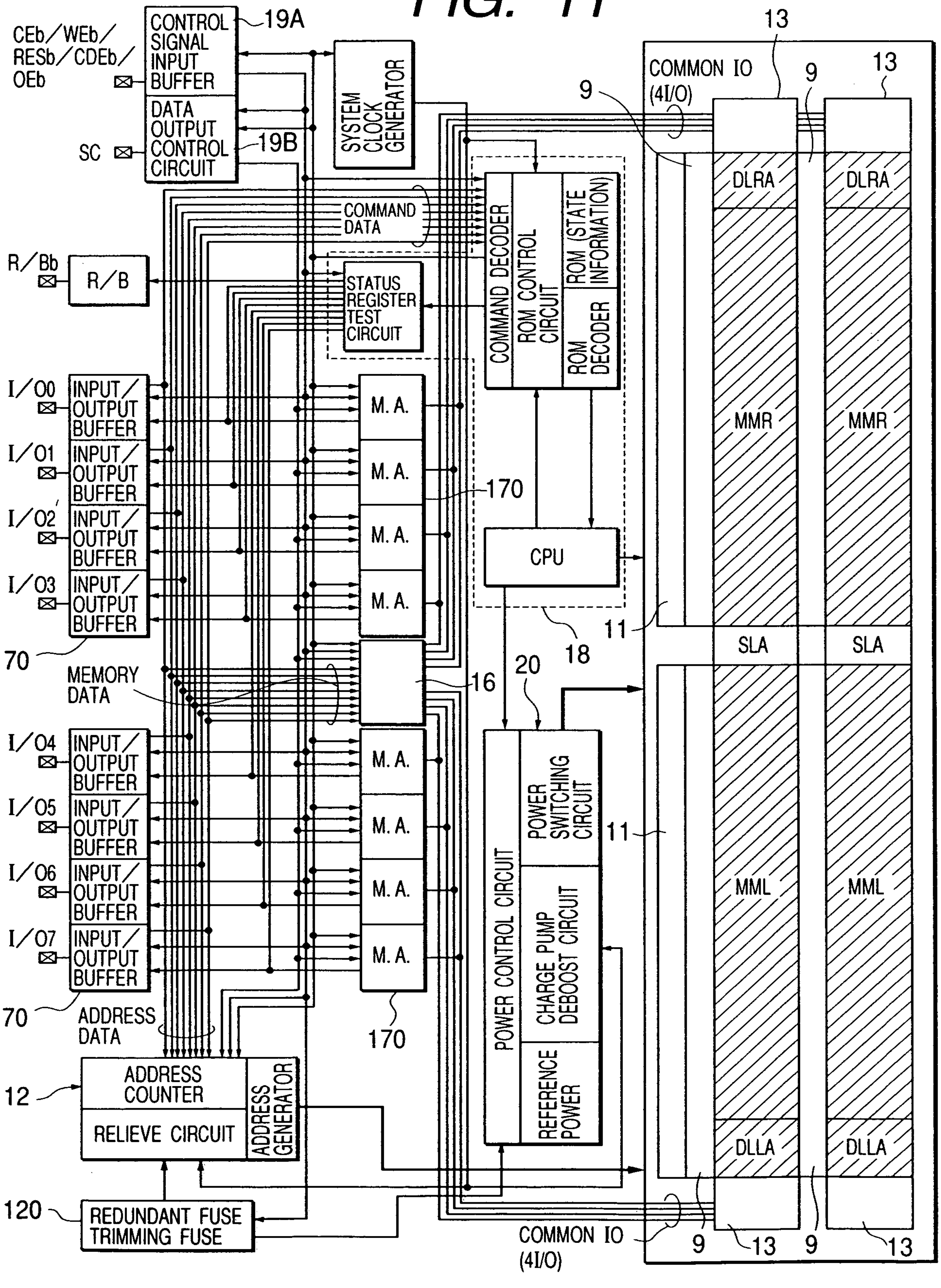
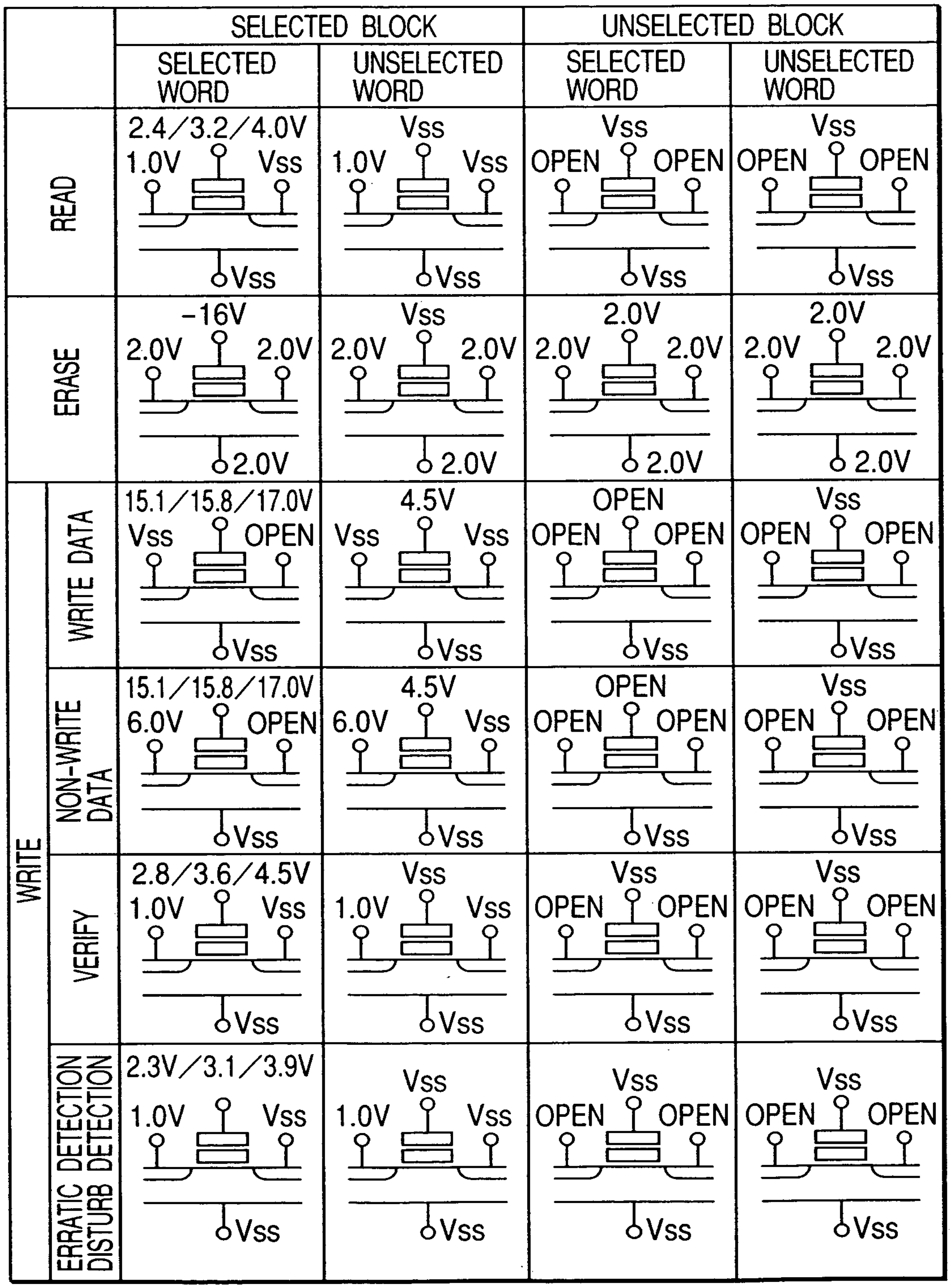

CEb/WEb/
RESb/CDEb/
OEb
CONTROL SIGNAL INPUT BUFFER
19A
DATA OUTPUT CONTROL CIRCUIT
19B
SC
SYSTEM CLOCK GENERATOR
COMMAND DATA
COMMAND DECODER
ROM CONTROL CIRCUIT
ROM (STATE INFORMATION)
ROM DECODER
R/Bb
R/B
STATUS REGISTER TEST CIRCUIT
I/O0
I/O1
I/O2
I/O3
I/O4
I/O5
I/O6
I/O7
INPUT/OUTPUT BUFFER
M. A.
170
CPU
18
70
MEMORY DATA
16
20
POWER CONTROL CIRCUIT
POWER SWITCHING CIRCUIT
CHARGE PUMP DEBOOST CIRCUIT
REFERENCE POWER
ADDRESS DATA
12
ADDRESS COUNTER
RELIEVE CIRCUIT
ADDRESS GENERATOR
120
REDUNDANT FUSE
TRIMMING FUSE
COMMON IO (4I/O)
13
9
11
DLRA
MMR
SLA
MML
DLLA

FIG. 12



		SELECTED BLOCK		UNSELECTED BLOCK	
		SELECTED WORD	UNSELECTED WORD	SELECTED WORD	UNSELECTED WORD
READ		2.4/3.2/4.0V 1.0V Vss Vss	Vss 1.0V Vss Vss	Vss OPEN OPEN Vss	Vss OPEN OPEN Vss
ERASE		-16V 2.0V 2.0V 2.0V	Vss 2.0V 2.0V 2.0V	2.0V 2.0V 2.0V 2.0V	2.0V 2.0V 2.0V 2.0V
WRITE	WRITE DATA	15.1/15.8/17.0V Vss OPEN Vss	4.5V Vss Vss Vss	OPEN OPEN OPEN Vss	Vss OPEN OPEN Vss
	NON-WRITE DATA	15.1/15.8/17.0V 6.0V OPEN Vss	4.5V 6.0V Vss Vss	OPEN OPEN OPEN Vss	Vss OPEN OPEN Vss
	VERIFY	2.8/3.6/4.5V 1.0V Vss Vss	Vss 1.0V Vss Vss	Vss OPEN OPEN Vss	Vss OPEN OPEN Vss
	ERRATIC DETECTION DISTURB DETECTION	2.3V/3.1/3.9V 1.0V Vss Vss	Vss 1.0V Vss Vss	Vss OPEN OPEN Vss	Vss OPEN OPEN Vss

FIG. 13

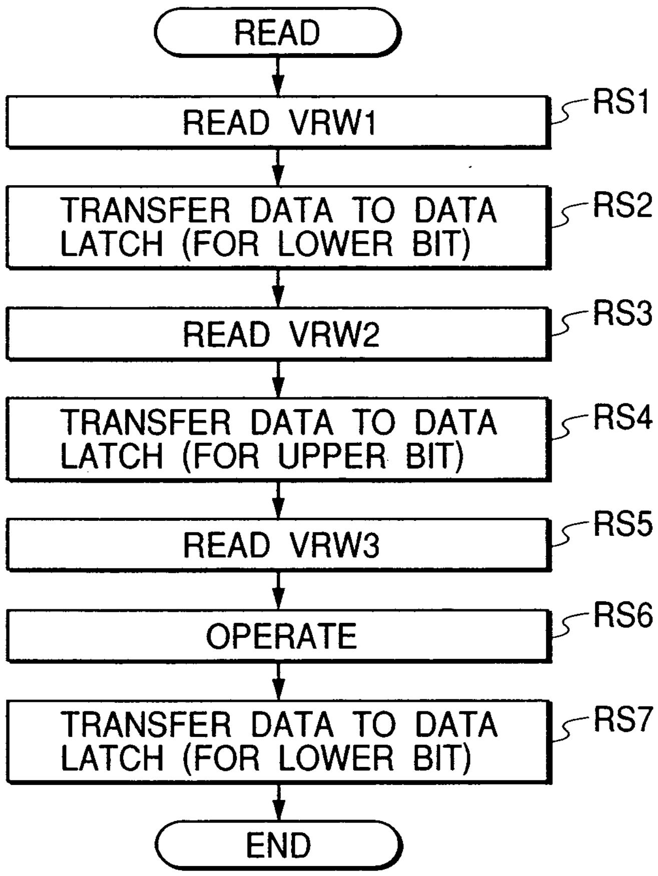

READ
READ VRW1
RS1
TRANSFER DATA TO DATA LATCH (FOR LOWER BIT)
RS2
READ VRW2
RS3
TRANSFER DATA TO DATA LATCH (FOR UPPER BIT)
RS4
READ VRW3
RS5
OPERATE
RS6
TRANSFER DATA TO DATA LATCH (FOR LOWER BIT)
RS7
END

FIG. 14

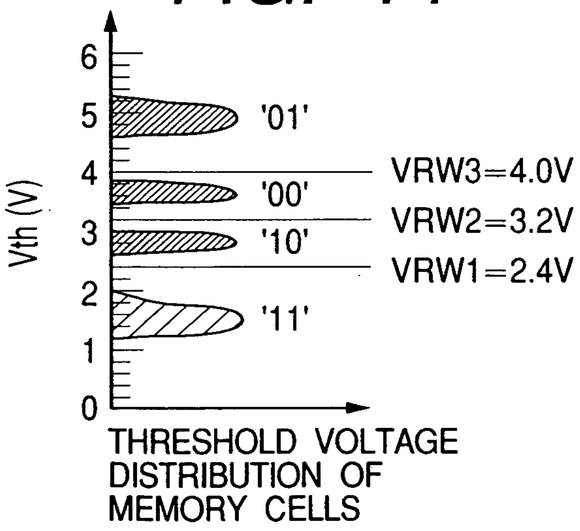

Vth (V)
6
5
4
3
2
1
0
'01'
'00'
'10'
'11'
VRW3=4.0V
VRW2=3.2V
VRW1=2.4V
THRESHOLD VOLTAGE DISTRIBUTION OF MEMORY CELLS

FIG. 15

WRITE/ADDITIONAL WRITE FLOW

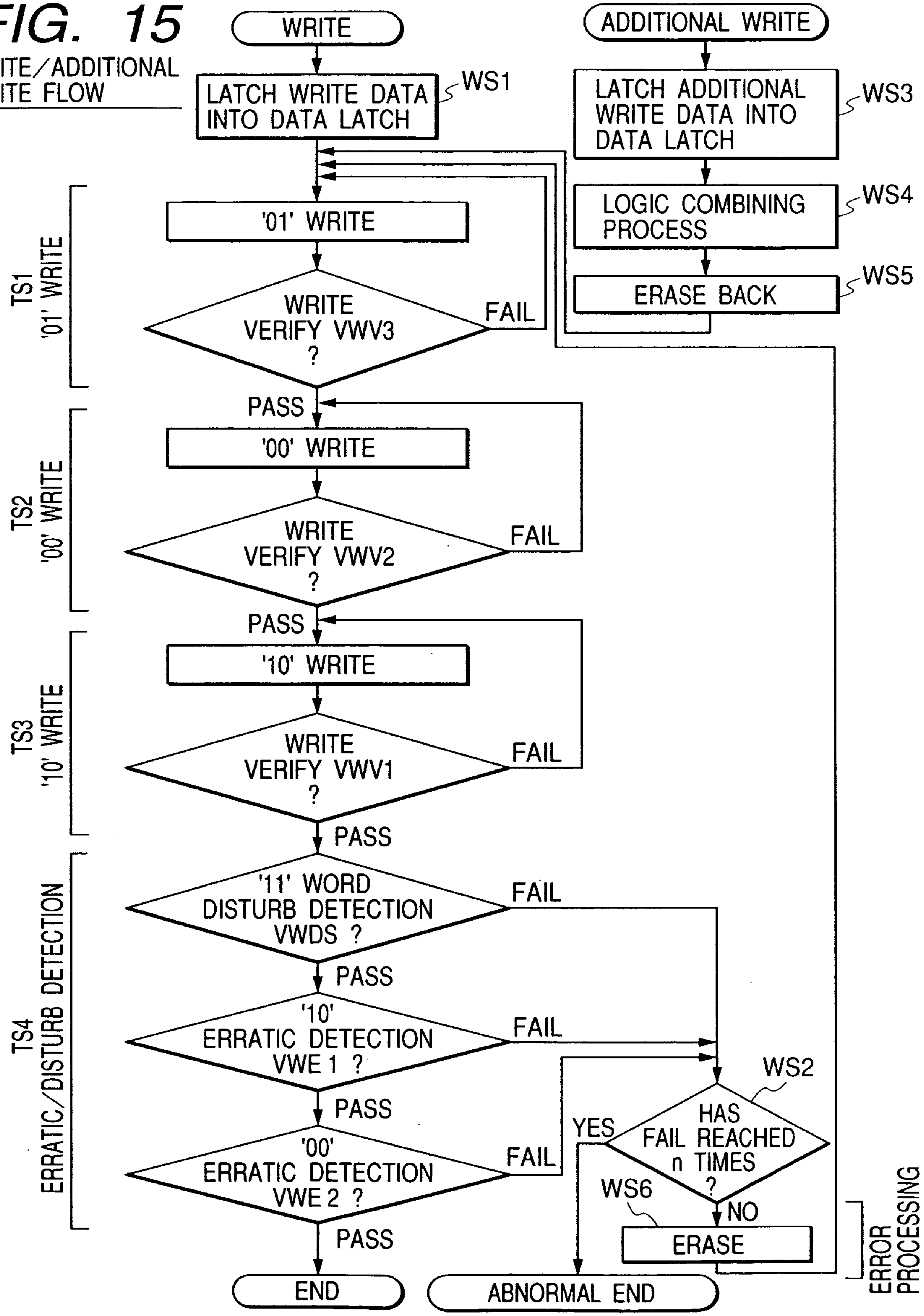


FIG. 16

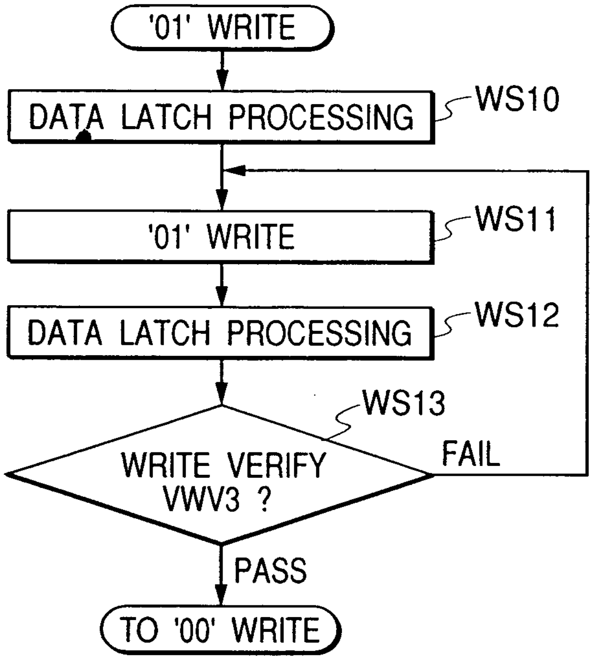

'01' WRITE
DATA LATCH PROCESSING
WS10
'01' WRITE
WS11
DATA LATCH PROCESSING
WS12
WS13
WRITE VERIFY VWV3 ?
FAIL
PASS
TO '00' WRITE

FIG. 17

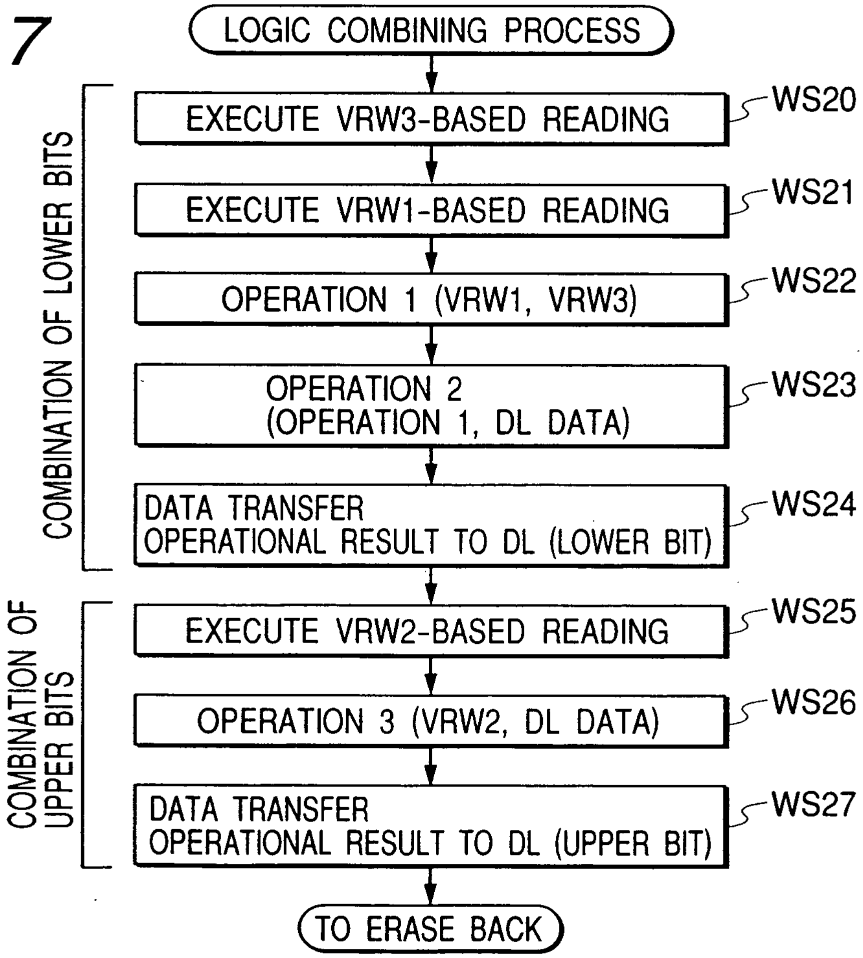

LOGIC COMBINING PROCESS
COMBINATION OF LOWER BITS
EXECUTE VRW3-BASED READING
WS20
EXECUTE VRW1-BASED READING
WS21
OPERATION 1 (VRW1, VRW3)
WS22
OPERATION 2 (OPERATION 1, DL DATA)
WS23
DATA TRANSFER OPERATIONAL RESULT TO DL (LOWER BIT)
WS24
COMBINATION OF UPPER BITS
EXECUTE VRW2-BASED READING
WS25
OPERATION 3 (VRW2, DL DATA)
WS26
DATA TRANSFER OPERATIONAL RESULT TO DL (UPPER BIT)
WS27
TO ERASE BACK

FIG. 18(A)

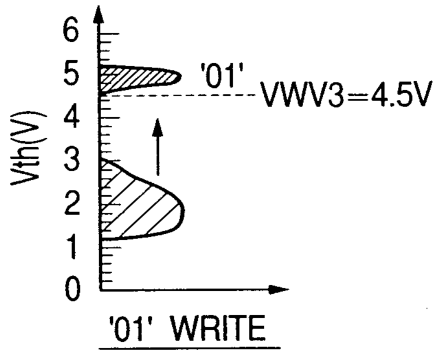


FIG. 18(B)

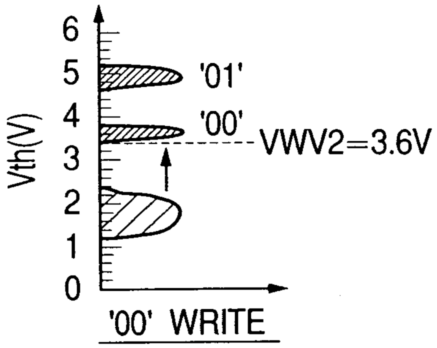


FIG. 18(C)

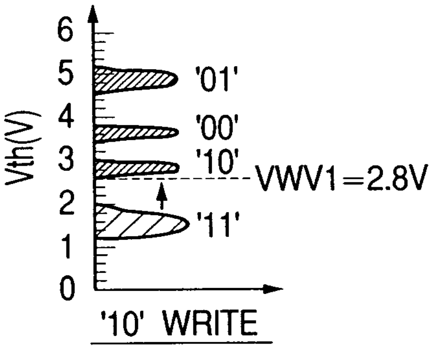


FIG. 18(D)

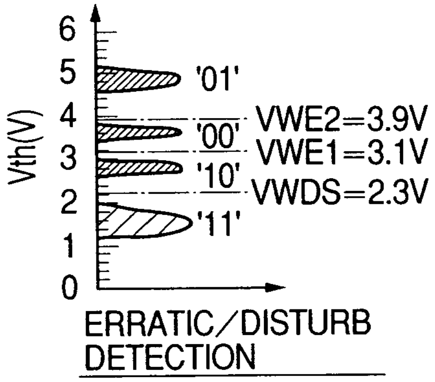


FIG. 18(E)

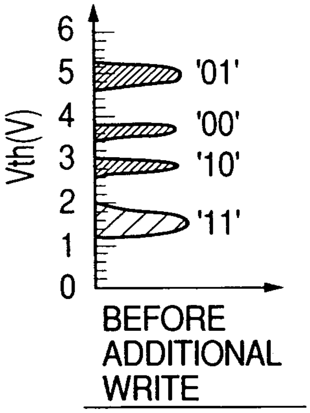


FIG. 18(F)

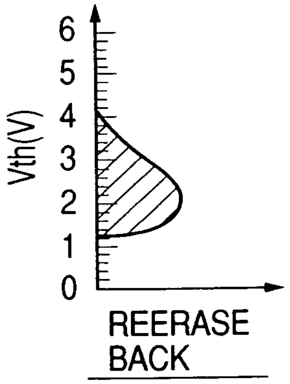


FIG. 19

ERASE FLOW

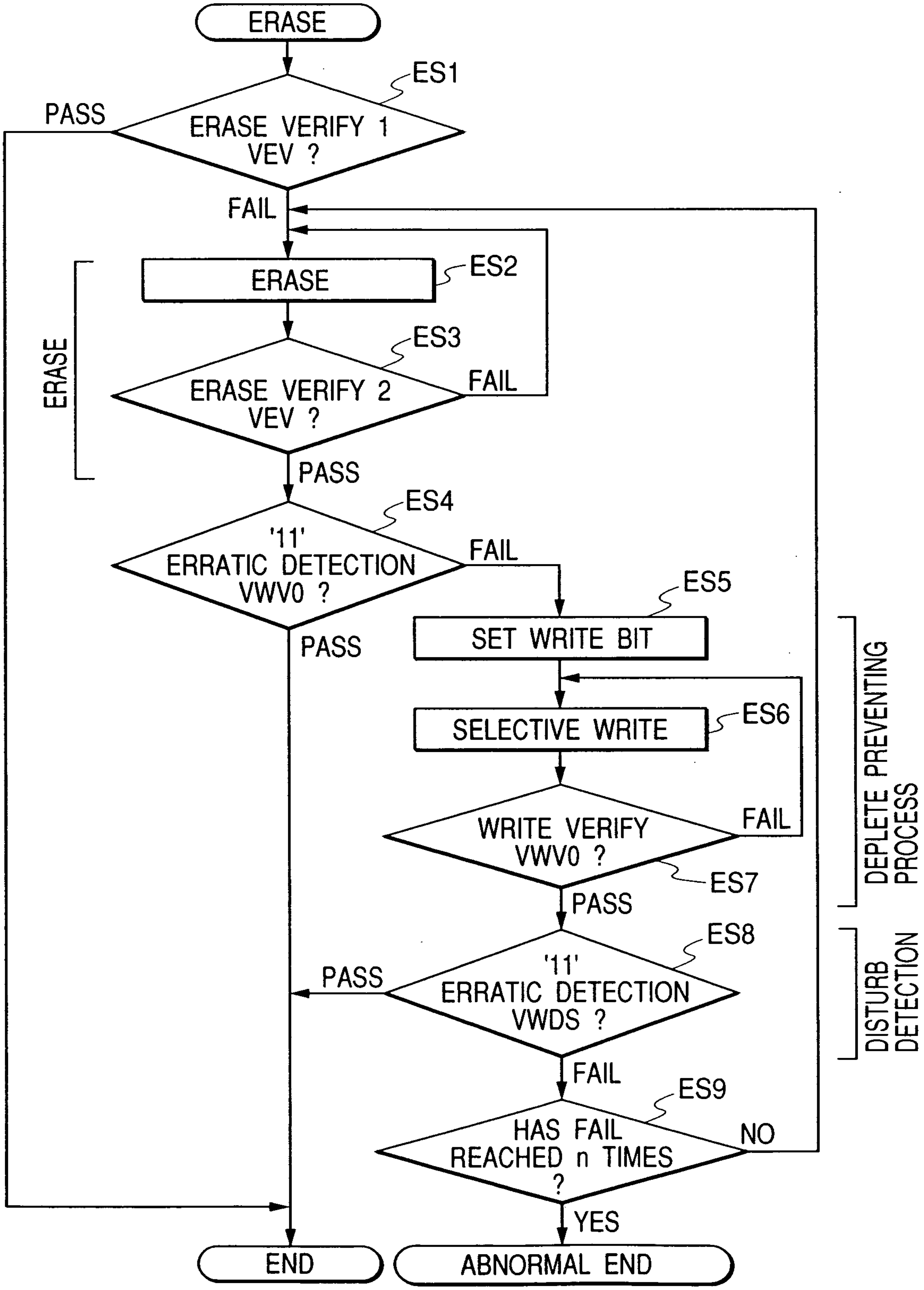


FIG. 20(A)

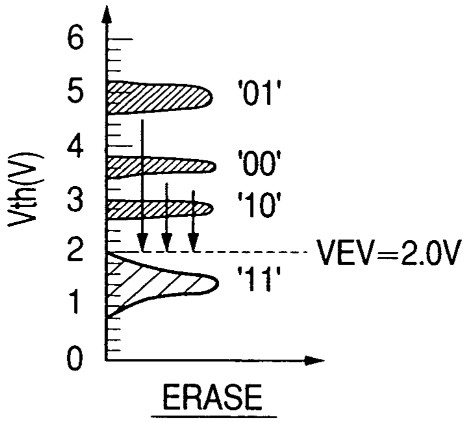


FIG. 20(B)

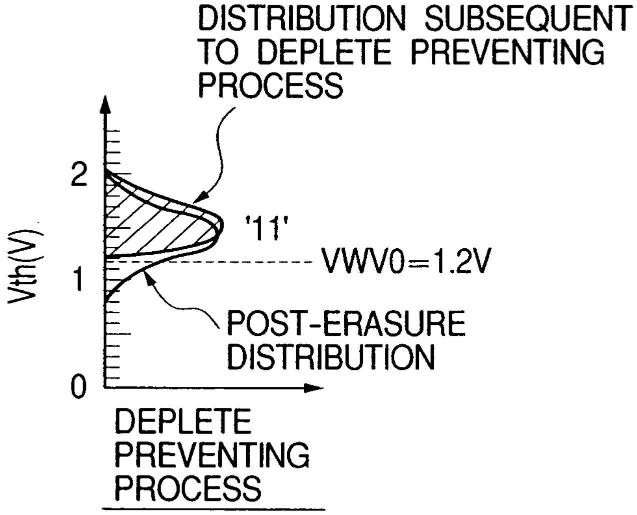


FIG. 21

DATA LATCH PROCESSING	CONTENTS OF OPERATION (SENSE LATCH DATA ON SELECTED MAT SIDE)
"01" WRITE DATA	$A+\overline{B}$
"00" WRITE DATA	$A+B$
"10" WRITE DATA	$\overline{A}+B$
"00" ERRATIC DETECTION DATA	$\overline{A+B}$
"10" ERRATIC DETECTION DATA	$A \cdot \overline{B}$
"11" DISTURB DETECTION DATA	$A \cdot B$

A : UPPER DATA   B : LOWER DATA

FIG. 22

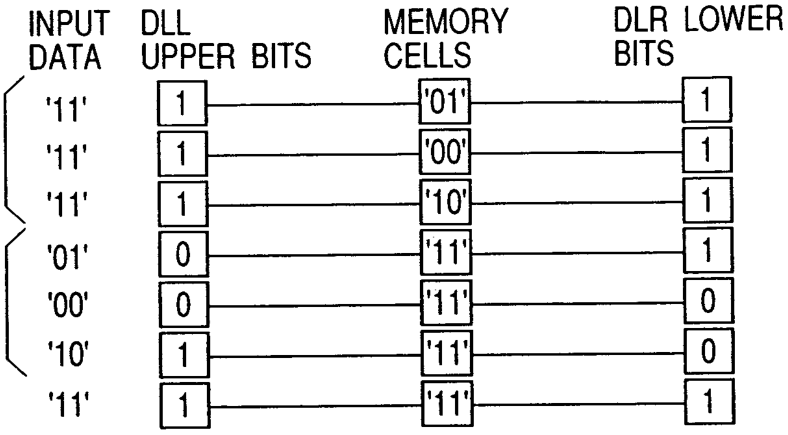
A UPPER	B LOWER	$A+\overline{B}$	$A+B$	$\overline{A}+B$	$\overline{A+B}$	$A \cdot \overline{B}$	$A \cdot B$
0	1	0	1	1	0	0	0
0	0	1	0	1	1	0	0
1	0	1	1	0	0	1	0
1	1	1	1	1	0	0	1

CONCEPT OF ADDITIONAL WRITING

FIG. 23(A)

INPUT '11' BECAUSE IT CANNOT BE WRITTEN IN ALREADY-WRITTEN UNIT

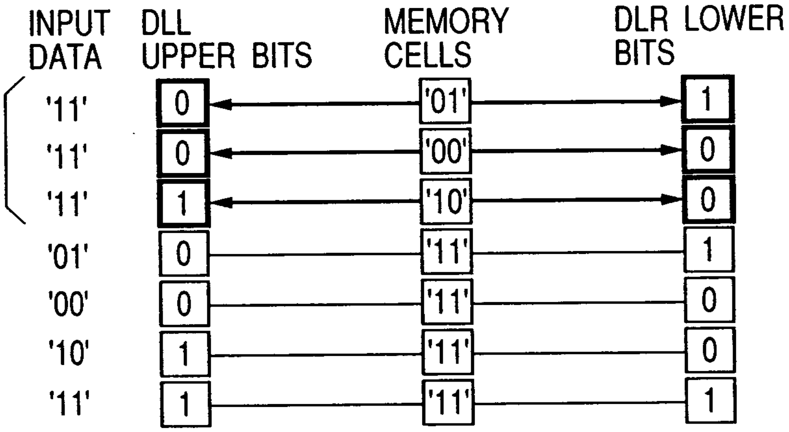
INPUT ADDITIONAL WRITE DATA ONLY WHEN MEMORY CELL IS IN ERASE STATE ('11')



(BEFORE LOGIC COMBINING PROCESS)

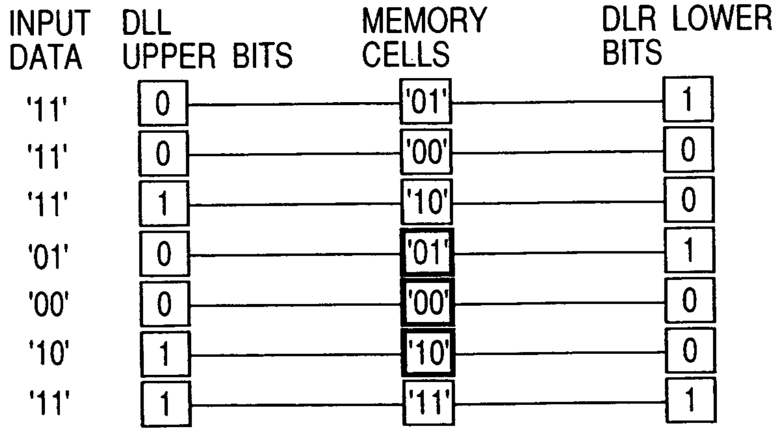
FIG. 23(B)

READ STATE OF MEMORY CELL AND STORE IT IN DATA LATCH



(AFTER LOGIC COMBINING PROCESS)

FIG. 23(C)



(AFTER ADDITIONAL WRITING)

FIG. 24

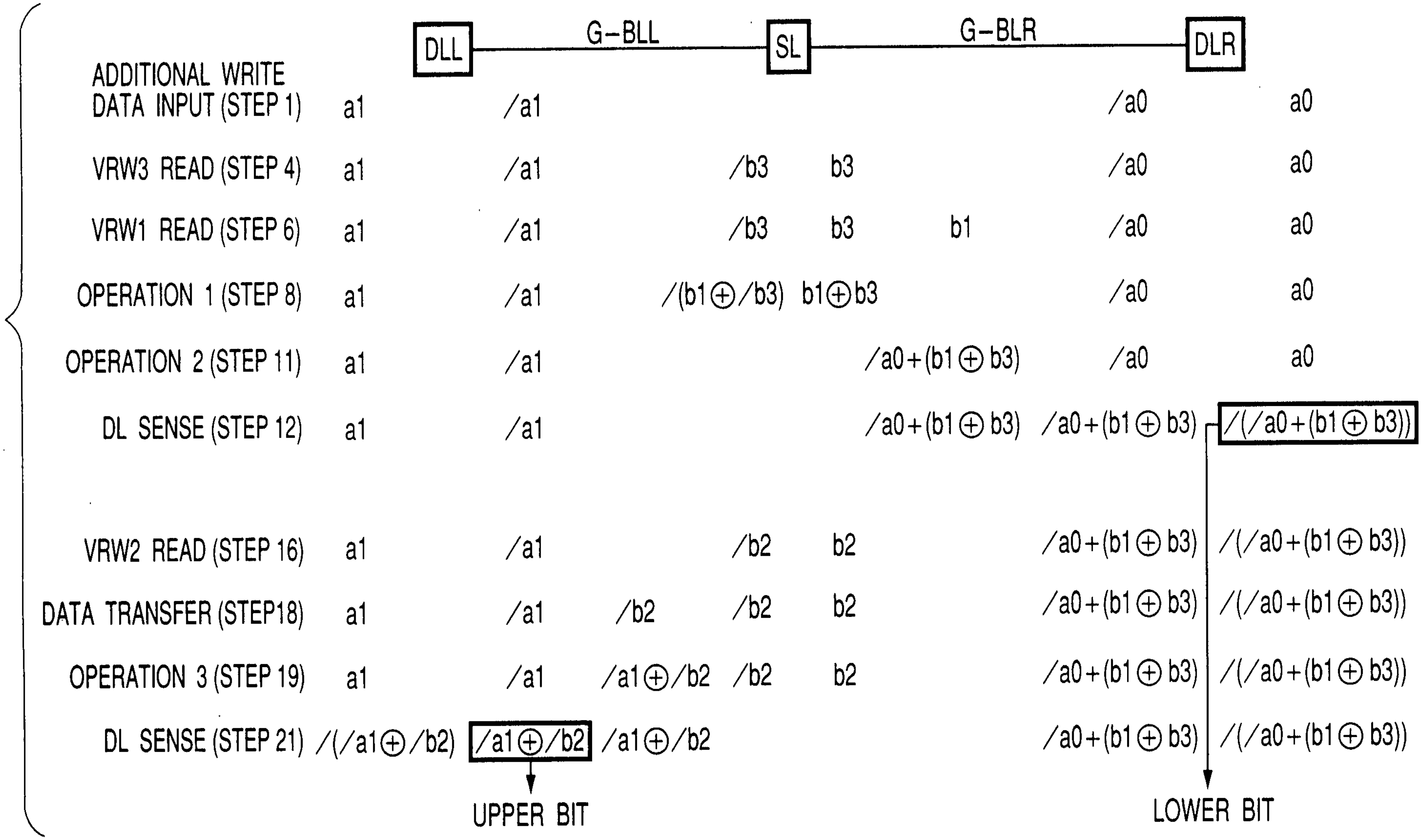
LOWER BIT : $a0 \cdot \overline{(b1 \oplus b3)}$

UPPER BIT : $\overline{a1} \oplus \overline{b2}$

a0 : ADDITIONAL WRITE DATA (LOWER BIT)
a1 : ADDITIONAL WRITE DATA (UPPER BIT)
b1 : MEMORY READ DATA (VRW1 (2.4V) READ)
b2 : MEMORY READ DATA (VRW2 (3.2V) READ)
b3 : MEMORY READ DATA (VRW3 (4.0V) READ)
$\oplus$: EXCLUSIVE OR

STATE OF MEMORY CELL	ADDITIONAL WRITE DATA	a1	a0	b1	b2	b3
01	11	1	1	1	1	1
00	11	1	1	1	1	0
10	11	1	1	1	0	0
11	01	0	1	0	0	0
11	00	0	0	0	0	0
11	10	1	0	0	0	0
11	11	1	1	0	0	0

FIG. 25



ADDITIONAL WRITE DATA INPUT (STEP 1)	a1	/a1				/a0	a0
VRW3 READ (STEP 4)	a1	/a1	/b3	b3		/a0	a0
VRW1 READ (STEP 6)	a1	/a1	/b3	b3	b1	/a0	a0
OPERATION 1 (STEP 8)	a1	/a1	/(b1⊕/b3)	b1⊕b3		/a0	a0
OPERATION 2 (STEP 11)	a1	/a1			/a0+(b1⊕b3)	/a0	a0
DL SENSE (STEP 12)	a1	/a1			/a0+(b1⊕b3)	/a0+(b1⊕b3)	/(/a0+(b1⊕b3))
VRW2 READ (STEP 16)	a1	/a1	/b2	b2		/a0+(b1⊕b3)	/(/a0+(b1⊕b3))
DATA TRANSFER (STEP18)	a1	/a1 /b2	/b2	b2		/a0+(b1⊕b3)	/(/a0+(b1⊕b3))
OPERATION 3 (STEP 19)	a1	/a1 /a1⊕/b2	/b2	b2		/a0+(b1⊕b3)	/(/a0+(b1⊕b3))
DL SENSE (STEP 21)	/(/a1⊕/b2)	/a1⊕/b2 /a1⊕/b2				/a0+(b1⊕b3)	/(/a0+(b1⊕b3))

FIG. 26

READ SEQUENCE

STEP	VRW1 READ												VRW2 READ											
	STEP 1						STEP 2						STEP 3						STEP 4					
CONTENTS	VRW1 READ						SL(R) → DLR DATA TRANSFER						VRW2 READ						SL(L) → DLL DATA TRANSFER					
	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR
01		0	0	1	1			0	0	1	1	1		0	0	1	1	1	0	0	0	1	1	1
00		0	0	1	1			0	0	1	1	1		0	0	1	1	1	0	0	0	1	1	1
10		0	0	1	1			0	0	1	1	1		1	1	0	0	1	1	1	1	0	0	1
11		1	1	0	0			1	1	0	0	0		1	1	0	0	0	1	1	1	0	0	0

VRW3 READ & OPERATION																																			
STEP 5						STEP 6						STEP 7						STEP 8						STEP 9						STEP 10					
VRW3 READ						G-BLL/R CLEAR						DLR → G-BLR DATA TRANSFER						OPERATION (SL(R), G-BLR)						DLR DATA CLEAR						G-BLR → DLR DATA TRANSFER (DLR SENSE)					
DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR
0	0	0	1	1	1	0	0	0	1	0	1	0	0	0	1	1	1	0	0	0	1	0	1	0	0	0	1	0	0	(1)0	0	0	1	0	(0)1
0	1	1	0	0	1	0	0	1	0	0	1	0	0	1	0	1	1	0	0	1	0	1	1	0	0	1	0	1	0	(1)0	0	1	0	1	(1)0
1	1	1	0	0	1	1	0	1	0	0	1	1	0	1	0	1	1	1	0	1	0	1	1	1	0	1	0	1	0	(0)1	0	1	0	1	(1)0
1	1	1	0	0	0	1	0	1	0	0	0	1	0	1	0	0	0	1	0	1	0	0	0	1	0	1	0	0	0	(0)1	0	1	0	0	(0)1

FIG. 27

WRITE SEQUENCE
(1) '01' WRITE

STEP	DATA INPUT						'01' WRITE DATA LATCH																	
	STEP 1						STEP 2						STEP 3						STEP 4					
CONTENTS	DATA INPUT						DATA TRANSFER DLR → G-BLR G-BLL PRECHARGE						SL SENSE						G-BLL/R DISCHARGE DATA TRANSFER SL(L) → G-BLL					
	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR
01	(1)0					(0)1	(1)0	0.5			0.0	(0)1	(1)0	1	1	0	0	(0)1	(1)0	1.0	1	0	0	(0)1
00	(1)0					(1)0	(1)0	0.5			1.0	(1)0	(1)0	0	0	1	1	(1)0	(1)0	0.0	0	1	0	(1)0
10	(0)1					(1)0	(0)1	0.5			1.0	(1)0	(0)1	0	0	1	1	(1)0	(0)1	0.0	0	1	0	(1)0
11	(0)1					(0)1	(0)1	0.5			0.0	(0)1	(0)1	1	1	0	0	(0)1	(0)1	1.0	1	0	0	(0)1

STEP	'01' WRITE DATA LATCH																	
	STEP 5						STEP 6						STEP 7					
CONTENTS	OPERATION (DLL, G-BLL) SL CLEAR						G-BLR PRECHARGE						SL SENSE					
	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR
01	(1)0	1.0	0	0	0	(0)1	(1)0	1.0	0	0	0.5	(0)1	(1)0	1	1	0	0	(0)1
00	(1)0	0.0	0	0	0	(1)0	(1)0	0.0	0	0	0.5	(1)0	(1)0	0	0	1	1	(1)0
10	(0)1	0.0	0	0	0	(1)0	(0)1	0.0	0	0	0.5	(1)0	(0)1	0	0	1	1	(1)0
11	(0)1	0.0	0	0	0	(0)1	(0)1	0.0	0	0	0.5	(0)1	(0)1	0	0	1	1	(0)1

(a) (b) (c) (d) (e) (f) (g) (h) (i) (j)

'01' WRITE						'01' WRITE VERIFY											
STEP 8						STEP 9						STEP 10					
WRITE						G-BLL/R DISCHARGE G-BLL/R PRECHARGE						MEMORY DISCHARGE (VWV3)					
DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR
(1)0	6.0	6.0	0.0	0.0	(0)1	(1)0	0.5	1	0	1.0	(0)1	(1)0	0.5	1	0	1.0	(0)1
(1)0	0.0	0.0	6.0	6.0	(1)0	(1)0	0.5	0	1	1.0	(1)0	(1)0	0.5	0	1	0.0	(1)0
(0)1	0.0	0.0	6.0	6.0	(1)0	(0)1	0.5	0	1	1.0	(1)0	(0)1	0.5	0	1	0.0	(1)0
(0)1	0.0	0.0	6.0	6.0	(0)1	(0)1	0.5	0	1	1.0	(0)1	(0)1	0.5	0	1	0.0	(0)1

'01' WRITE VERIFY																	
STEP 11						STEP 12						STEP 13					
UNSELECTED G-BLR PRECHARGE						SL CLEAR SL SENSE & ALL DETERMINATION						G-BLL/R DISCHARGE SL CLEAR					
DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR
(1)0	0.5	1	0	1.0	(0)1	(1)0	0.5	0	1	1.0	(0)1	(1)0	0.0	0	0	0.0	(0)1
(1)0	0.5	0	1	1.0	(1)0	(1)0	0.5	0	1	1.0	(1)0	(1)0	0.0	0	0	0.0	(1)0
(0)1	0.5	0	1	1.0	(1)0	(0)1	0.5	0	1	1.0	(1)0	(0)1	0.0	0	0	0.0	(1)0
(0)1	0.5	0	1	1.0	(0)1	(0)1	0.5	0	1	1.0	(0)1	(0)1	0.0	0	0	0.0	(0)1

ALL DETERMINATION: TO STEP 8 IF FAIL IS REACHED

FIG. 28

(2) '00' WRITE

STEP	'00' WRITE DATA LATCH																																			
	STEP 14						STEP 15						STEP 16						STEP 17						STEP 18						STEP 19					
CONTENTS	DATA TRANSFER DLR →G-BLR G-BLL PRECHARGE						SL SENSE						G-BLL/R DISCHARGE G-BLL/R PRECHARGE						OPERATION (G-BLL, SL(L))						OPERATION (DLL, G-BLL) SL CLEAR						SL SENSE					
	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR
01	(1)0	0.5			0.0	(0)1	(1)0	1	1	0	0	(0)1	(1)0	1.0	1	0	0.5	(0)1	(1)0	0.0	1	0	0.5	(0)1	(1)0	0.0	0	0	0.5	(0)1	(1)0	0	0	1	1	(0)1
00	(1)0	0.5			1.0	(1)0	(1)0	0	0	1	1	(1)0	(1)0	1.0	0	1	0.5	(1)0	(1)0	1.0	0	1	0.5	(1)0	(1)0	1.0	0	0	0.5	(1)0	(1)0	1	1	0	0	(1)0
10	(0)1	0.5			1.0	(1)0	(0)1	0	0	1	1	(1)0	(0)1	1.0	0	1	0.5	(1)0	(0)1	1.0	0	1	0.5	(1)0	(0)1	0.0	0	0	0.5	(1)0	(0)1	0	0	1	1	(1)0
11	(0)1	0.5			0.0	(0)1	(0)1	1	1	0	0	(0)1	(0)1	1.0	1	0	0.5	(0)1	(0)1	0.0	1	0	0.5	(0)1	(0)1	0.0	0	0	0.5	(0)1	(0)1	0	0	1	1	(0)1

'00' WRITE						'00' WRITE VERIFY																													
STEP 20						STEP 21						STEP 22						STEP 23						STEP 24						STEP 25					
WRITE						G-BLL/R DISCHARGE G-BLL/R PRECHARGE						MEMORY DISCHARGE (VWV2)						UNSELECTED G-BLR PRECHARGE						SL CLEAR SL SENSE & ALL DETERMINATION						G-BLL/R DISCHARGE SL CLEAR					
DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR
(1)0	0.0	0.0	6.0	6.0	(0)1	(1)0	0.5	0	1	1.0	(0)1	(1)0	0.5	0	1	1.0	(0)1	(1)0	0.5	0	1	1.0	(0)1	(1)0	0.5	0	1	1.0	(0)1	(1)0	0.0	0	0	0.0	(0)1
(1)0	6.0	6.0	0.0	0.0	(1)0	(1)0	0.5	1	0	1.0	(1)0	(1)0	0.5	1	0	1.0	(1)0	(1)0	0.5	1	0	1.0	(1)0	(1)0	0.5	0	1	1.0	(1)0	(1)0	0.0	0	0	0.0	(1)0
(0)1	0.0	0.0	6.0	6.0	(1)0	(0)1	0.5	0	1	1.0	(1)0	(0)1	0.5	0	1	0.0	(1)0	(0)1	0.5	0	1	1.0	(1)0	(0)1	0.5	0	1	1.0	(1)0	(0)1	0.0	0	0	0.0	(1)0
(0)1	0.0	0.0	6.0	6.0	(0)1	(0)1	0.5	0	1	1.0	(0)1	(0)1	0.5	0	1	0.0	(0)1	(0)1	0.5	0	1	1.0	(0)1	(0)1	0.5	0	1	1.0	(0)1	(0)1	0.0	0	0	0.0	(0)1

ALL DETERMINATION: TO STEP 20 IF FAIL IS REACHED

FIG. 29

(3) '10' WRITE

STEP	'10' WRITE DATA LATCH																																			
	STEP 26						STEP 27						STEP 28						STEP 29						STEP 30						STEP 31					
CONTENTS	DATA TRANSFER DLR → G-BLR G-BLL PRECHARGE						SL SENSE						G-BLL/R DISCHARGE DATA TRANSFER DLL → G-BLL						OPERATION (G-BLL, SL(L))						SL CLEAR G-BLR PRECHARGE						SL SENSE					
	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR
01	(1)0	0.5			0.0	(0)1	(1)0	1	1	0	0	(0)1	(1)0	0.0	1	0	0	(0)1	(1)0	0.0	1	0	0	(0)1	(1)0	0.0	0	0	0.5	(0)1	(1)0	0	0	1	1	(0)1
00	(1)0	0.5			1.0	(1)0	(1)0	0	0	1	1	(1)0	(1)0	0.0	0	1	0	(1)0	(1)0	0.0	0	1	0	(1)0	(1)0	0.0	0	0	0.5	(1)0	(1)0	0	0	1	1	(1)0
10	(0)1	0.5			1.0	(1)0	(0)1	0	0	1	1	(1)0	(0)1	1.0	0	1	0	(1)0	(0)1	1.0	0	1	0	(1)0	(0)1	1.0	0	0	0.5	(1)0	(0)1	1	1	0	0	(1)0
11	(0)1	0.5			0.0	(0)1	(0)1	1	1	0	0	(0)1	(0)1	1.0	1	0	0	(0)1	(0)1	0.0	1	0	0	(0)1	(0)1	0.0	0	0	0.5	(0)1	(0)1	0	0	1	1	(0)1

'10' WRITE						'10' WRITE VERIFY																													
STEP 32						STEP 33						STEP 34						STEP 35						STEP 36						STEP 37					
WRITE						G-BLL/R DISCHARGE G-BLL/R PRECHARGE						MEMORY DISCHARGE (VWV1)						UNSELECTED G-BLR PRECHARGE						SL CLEAR SL SENSE & ALL DETERMINATION						G-BLL/R DISCHARGE SL CLEAR					
DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR
(1)0	0.0	0.0	6.0	6.0	(0)1	(1)0	0.5	0	1	1.0	(0)1	(1)0	0.5	0	1	1.0	(0)1	(1)0	0.5	0	1	1.0	(0)1	(1)0	0.5	0	1	1.0	(0)1	(1)0	0.0	0	0	0.0	(0)1
(1)0	0.0	0.0	6.0	6.0	(1)0	(1)0	0.5	0	1	1.0	(1)0	(1)0	0.5	0	1	1.0	(1)0	(1)0	0.5	0	1	1.0	(1)0	(1)0	0.5	0	1	1.0	(1)0	(1)0	0.0	0	0	0.0	(1)0
(0)1	6.0	6.0	0.0	0.0	(1)0	(0)1	0.5	1	0	1.0	(1)0	(0)1	0.5	1	0	1.0	(1)0	(0)1	0.5	1	0	1.0	(1)0	(0)1	0.5	0	1	1.0	(1)0	(0)1	0.0	0	0	0.0	(1)0
(0)1	0.0	0.0	6.0	6.0	(0)1	(0)1	0.5	0	1	1.0	(0)1	(0)1	0.5	0	1	0.0	(0)1	(0)1	0.5	0	1	1.0	(0)1	(0)1	0.5	0	1	1.0	(0)1	(0)1	0.0	0	0	0.0	(0)1

ALL DETERMINATION: TO STEP 32 IF FAIL IS REACHED

FIG. 30

(4) '11' WORD DISTURB DETECTION

STEP	'11' WORD DISTURB DATA LATCH																																			
	STEP 38						STEP 39						STEP 40						STEP 41						STEP 42						STEP 43					
CONTENTS	DATA TRANSFER DLL → G-BLL G-BLR PRECHARGE						SL SENSE						G-BLL/R DISCHARGE G-BLL/R PRECHARGE						OPERATION (SL(R), G-BLR)						OPERATION (G-BLR, DLR) SL CLEAR						SL SENSE					
	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR
01	(1)0	0.0			0.5	(0)1	(1)0	0	0	1	1	(0)1	(1)0	0.5	0	1	1.0	(0)1	(1)0	0.5	0	1	0.0	(0)1	(1)0	0.5	0	0	0.0	(0)1	(1)0	1	1	0	0	(0)1
00	(1)0	0.0			0.5	(1)0	(1)0	0	0	1	1	(1)0	(1)0	0.5	0	1	1.0	(1)0	(1)0	0.5	0	1	0.0	(1)0	(1)0	0.5	0	0	0.0	(1)0	(1)0	1	1	0	0	(1)0
10	(0)1	1.0			0.5	(1)0	(0)1	1	1	0	0	(1)0	(0)1	0.5	1	0	1.0	(1)0	(0)1	0.5	1	0	1.0	(1)0	(0)1	0.5	0	0	0.0	(1)0	(0)1	1	1	0	0	(1)0
11	(0)1	1.0			0.5	(0)1	(0)1	1	1	0	0	(0)1	(0)1	0.5	1	0	1.0	(0)1	(0)1	0.5	1	0	1.0	(0)1	(0)1	0.5	0	0	1.0	(0)1	(0)1	0	0	1	1	(0)1

'11' WORD DISTURB DETECTION																													
STEP 44						STEP 45						STEP 46						STEP 47						STEP 48					
G-BLL/R DISCHARGE						G-BLR SELECT PRECHARGE G-BLL PRECHARGE						MEMORY DISCHARGE (VWDS)						SL CLEAR SL SENSE & ALL DETERMINATION						G-BLL/R DISCHARGE SL CLEAR					
DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR
(1)0	0	1	0	0	(0)1	(1)0	0.5	1	0	0.0	(0)1	(1)0	0.5	1	0	0.0	(0)1	(1)0	0.5	1	0	0.0	(0)1	(1)0	0.0	0	0	0.0	(0)1
(1)0	0	1	0	0	(1)0	(1)0	0.5	1	0	0.0	(1)0	(1)0	0.5	1	0	0.0	(1)0	(1)0	0.5	1	0	0.0	(1)0	(1)0	0.0	0	0	0.0	(1)0
(0)1	0	1	0	0	(1)0	(0)1	0.5	1	0	0.0	(1)0	(0)1	0.5	1	0	0.0	(1)0	(0)1	0.5	1	0	0.0	(1)0	(0)1	0.0	0	0	0.0	(1)0
(0)1	0	0	1	0	(0)1	(0)1	0.5	0	1	1.0	(0)1	(0)1	0.5	0	1	0.0	(0)1	(0)1	0.5	1	0	0.0	(0)1	(0)1	0.0	0	0	0.0	(0)1

ALL DETERMINATION: TO ERASE IF FAIL IS REACHED

FIG. 31

(5) '10' ERRATIC DETECTION

STEP	'10' ERRATIC DATA LATCH																																			
	STEP 49						STEP 50						STEP 51						STEP 52						STEP 53						STEP 54					
CONTENTS	DATA TRANSFER DLL → G-BLL G-BLR PRECHARGE						SL SENSE						G-BLL/R DISCHARGE DATA TRANSFER DLR → G-BLR						OPERATION (SL(R), G-BLR)						SL CLEAR G-BLL PRECHARGE						SL SENSE					
	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR
01	(1)0	0.0			0.5	(0)1	(1)0	0	0	1	1	(0)1	(1)0	0	0	1	0.0	(0)1	(1)0	0	0	1	0.0	(0)1	(1)0	0.5	0	0	0.0	(0)1	(1)0	1	1	0	0	(0)1
00	(1)0	0.0			0.5	(1)0	(1)0	0	0	1	1	(1)0	(1)0	0	0	1	1.0	(1)0	(1)0	0	0	1	0.0	(1)0	(1)0	0.5	0	0	0.0	(1)0	(1)0	1	1	0	0	(1)0
10	(0)1	1.0			0.5	(1)0	(0)1	1	1	0	0	(1)0	(0)1	0	1	0	1.0	(1)0	(0)1	0	1	0	1.0	(1)0	(0)1	0.5	0	0	1.0	(1)0	(0)1	0	0	1	1	(1)0
11	(0)1	1.0			0.5	(0)1	(0)1	1	1	0	0	(0)1	(0)1	0	1	0	0.0	(0)1	(0)1	0	1	0	0.0	(0)1	(0)1	0.5	0	0	0.0	(0)1	(0)1	1	1	0	0	(0)1

'10' ERRATIC DETECTION																													
STEP 55						STEP 56						STEP 57						STEP 58						STEP 59					
G-BLL/R DISCHARGE						G-BLR SELECT PRECHARGE G-BLL PRECHARGE						MEMORY DISCHARGE (VWE1)						SL CLEAR SL SENSE & ALL DETERMINATION						G-BLL/R DISCHARGE SL CLEAR					
DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR
(1)0	0	1	0	0	(0)1	(1)0	0.5	1	0	0.0	(0)1	(1)0	0.5	1	0	0.0	(0)1	(1)0	0.5	1	0	0.0	(0)1	(1)0	0.0	0	0	0.0	(0)1
(1)0	0	1	0	0	(1)0	(1)0	0.5	1	0	0.0	(1)0	(1)0	0.5	1	0	0.0	(1)0	(1)0	0.5	1	0	0.0	(1)0	(1)0	0.0	0	0	0.0	(1)0
(0)1	0	0	1	0	(1)0	(0)1	0.5	0	1	1.0	(1)0	(0)1	0.5	0	1	0.0	(1)0	(0)1	0.5	1	0	0.0	(1)0	(0)1	0.0	0	0	0.0	(1)0
(0)1	0	1	0	0	(0)1	(0)1	0.5	1	0	0.0	(0)1	(0)1	0.5	1	0	0.0	(0)1	(0)1	0.5	1	0	0.0	(0)1	(0)1	0.0	0	0	0.0	(0)1

ALL DETERMINATION: TO ERASE IF FAIL IS REACHED

FIG. 32

(6) '00' ERRATIC DETECTION

STEP	'00' ERRATIC DATA LATCH																																			
	STEP 60						STEP 61						STEP 62						STEP 63						STEP 64						STEP 65					
CONTENTS	DATA TRANSFER DLR→G-BLR G-BLL PRECHARGE						SL SENSE						G-BLL/R DISCHARGE DATA TRANSFER SL(L) →G-BLL						OPERATION (DLL, G-BLL)						SL CLEAR G-BLR PRECHARGE						SL SENSE					
	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR
01	(1)0	0.5			0.0	(0)1	(1)0	1	1	0	0	(0)1	(1)0	1.0	1	0	0	(0)1	(1)0	1.0	1	0	0	(0)1	(1)0	1.0	0	0	0.5	(0)1	(1)0	1	1	0	0	(0)1
00	(1)0	0.5			1.0	(1)0	(1)0	0	0	1	1	(1)0	(1)0	0.0	0	1	0	(1)0	(1)0	0.0	0	1	0	(1)0	(1)0	0.0	0	0	0.5	(1)0	(1)0	0	0	1	1	(1)0
10	(0)1	0.5			1.0	(1)0	(0)1	0	0	1	1	(1)0	(0)1	0.0	0	1	0	(1)0	(0)1	1.0	0	1	0	(1)0	(0)1	1.0	0	0	0.5	(1)0	(0)1	1	1	0	0	(1)0
11	(0)1	0.5			0.0	(0)1	(0)1	1	1	0	0	(0)1	(0)1	1.0	1	0	0	(0)1	(0)1	1.0	1	0	0	(0)1	(0)1	1.0	0	0	0.5	(0)1	(0)1	1	1	0	0	(0)1

'00' ERRATIC DETECTION																													
STEP 66						STEP 67						STEP 68						STEP 69						STEP 70					
G-BLL/R DISCHARGE						G-BLR SELECT PRECHARGE G-BLL PRECHARGE						MEMORY DISCHARGE (VWE2)						SL CLEAR SL SENSE & ALL DETERMINATION						G-BLL/R DISCHARGE SL CLEAR					
DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR
(1)0	0	1	0	0	(0)1	(1)0	0.5	1	0	0.0	(0)1	(1)0	0.5	1	0	0.0	(0)1	(1)0	0.5	1	0	0.0	(0)1	(1)0	0.0	0	0	0.0	(0)1
(1)0	0	0	1	0	(1)0	(1)0	0.5	0	1	1.0	(1)0	(1)0	0.5	0	1	0.0	(1)0	(1)0	0.5	1	0	0.0	(1)0	(1)0	0.0	0	0	0.0	(1)0
(0)1	0	1	0	0	(1)0	(0)1	0.5	1	0	0.0	(1)0	(0)1	0.5	1	0	0.0	(1)0	(0)1	0.5	1	0	0.0	(1)0	(0)1	0.0	0	0	0.0	(1)0
(0)1	0	1	0	0	(0)1	(0)1	0.5	1	0	0.0	(0)1	(0)1	0.5	1	0	0.0	(0)1	(0)1	0.5	1	0	0.0	(0)1	(0)1	0.0	0	0	0.0	(0)1

ALL DETERMINATION: TO ERASE IF FAIL IS REACHED

FIG. 33

3. ADDITIONAL WRITE

STEP		COMBINATION OF LOWER BITS																																									
		STEP 1						STEP 2						STEP 3						STEP 4						STEP 5						STEP 6						STEP 7					
CONTENTS		DATA INPUT						G-BLL/R PRECHARGE						MEMORY DISCHARGE (VRW3)						SL SENSE						G-BLL/R DISCHARGE G-BLL/R PRECHARG						MEMORY DISCHARGE (VRW1)						OPERATION (SL(R), G-BLR)					
STATE OF MEMORY CELL	WRITE DATA	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR
01	11	1(0)					(0)1	1(0)	1			1.0	(0)1	1(0)	0.5			1.0	(0)1	1(0)	0	0	1	1	(0)1	1(0)	1	0	1	1.0	(0)1	1(0)	1	0	1	1.0	(0)1	1(0)	1	0	1	0.0	(0)1
00	11	1(0)					(0)1	1(0)	1			1.0	(0)1	1(0)	0.5			0.0	(0)1	1(0)	1	1	0	0	(0)1	1(0)	1	1	0	1.0	(0)1	1(0)	1	1	0	1.0	(0)1	1(0)	1	1	0	1.0	(0)1
10	11	1(0)					(0)1	1(0)	1			1.0	(0)1	1(0)	0.5			0.0	(0)1	1(0)	1	1	0	0	(0)1	1(0)	1	1	0	1.0	(0)1	1(0)	1	1	0	1.0	(0)1	1(0)	1	1	0	1.0	(0)1
11	01	0(1)					(0)1	0(1)	1			1.0	(0)1	0(1)	0.5			0.0	(0)1	0(1)	1	1	0	0	(0)1	0(1)	1	1	0	1.0	(0)1	0(1)	1	1	0	0.0	(0)1	0(1)	1	1	0	0.0	(0)1
	00	0(1)					(1)0	0(1)	1			1.0	(1)0	0(1)	0.5			0.0	(1)0	0(1)	1	1	0	0	(1)0	0(1)	1	1	0	1.0	(1)0	0(1)	1	1	0	0.0	(1)0	0(1)	1	1	0	0.0	(1)0
	10	1(0)					(1)0	1(0)	1			1.0	(1)0	1(0)	0.5			0.0	(1)0	1(0)	1	1	0	0	(1)0	1(0)	1	1	0	1.0	(1)0	1(0)	1	1	0	0.0	(1)0	1(0)	1	1	0	0.0	(1)0
	11	1(0)					(0)1	1(0)	1			1.0	(0)1	1(0)	0.5			0.0	(0)1	1(0)	1	1	0	0	(0)1	1(0)	1	1	0	1.0	(0)1	1(0)	1	1	0	0.0	(0)1	1(0)	1	1	0	0.0	(0)1

(a)

※ INPUT DATA OF UNSELECT SIDE DL IS THE INVERSE OF NORMAL WRITING

STEP 8						STEP 9						STEP 10						STEP 11						STEP 12						STEP 13					
SL CLEAR SL SENSE						G-BLL/R DISCHARGE						DATA TRANSFER (DLR → G-BLR) DATA TRANSFER (SL(R) → G-BLR)						SL CLEAR DLR CLEAR						DL SENSE						G-BLL/R DISCHARGE					
DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR
1(0)	1	1	0	0	(0)1	1(0)	0.0	1	0	0.0	(0)1	1(0)	0.0	1	0	0.0	(0)1	1(0)	0.0	0	0	0.0	0	1(0)	0.0	0	0	0.0	0(1)	1(0)	0.0	0	0	0.0	0(1)
1(0)	0	0	1	1	(0)1	1(0)	0.0	0	1	0.0	(0)1	1(0)	0.0	0	1	1.0	(0)1	1(0)	0.0	0	0	1.0	0	1(0)	0.0	0	0	1.0	1(0)	1(0)	0.0	0	0	0.0	1(0)
1(0)	0	0	1	1	(0)1	1(0)	0.0	0	1	0.0	(0)1	1(0)	0.0	0	1	1.0	(0)1	1(0)	0.0	0	0	1.0	0	1(0)	0.0	0	0	1.0	1(0)	1(0)	0.0	0	0	0.0	1(0)
0(1)	1	1	0	0	(0)1	0(1)	0.0	1	0	0.0	(0)1	0(1)	0.0	1	0	0.0	(0)1	0(1)	0.0	0	0	0.0	0	0(1)	0.0	0	0	0.0	0(1)	0(1)	0.0	0	0	0.0	0(1)
0(1)	1	1	0	0	(1)0	0(1)	0.0	1	0	0.0	(1)0	0(1)	0.0	1	0	1.0	(1)0	0(1)	0.0	0	0	1.0	0	0(1)	0.0	0	0	1.0	1(0)	0(1)	0.0	0	0	0.0	1(0)
1(0)	1	1	0	0	(1)0	1(0)	0.0	1	0	0.0	(1)0	1(0)	0.0	1	0	1.0	(1)0	1(0)	0.0	0	0	1.0	0	1(0)	0.0	0	0	1.0	1(0)	1(0)	0.0	0	0	0.0	1(0)
1(0)	1	1	0	0	(0)1	1(0)	0.0	1	0	0.0	(0)1	1(0)	0.0	1	0	0.0	(0)1	1(0)	0.0	0	0	0.0	0	1(0)	0.0	0	0	0.0	0(1)	1(0)	0.0	0	0	0.0	0(1)

FIG. 34

ADDITIONAL WRITE

STEP		COMBINATION OF UPPER BITS																																			
		STEP 14						STEP 15						STEP 16						STEP 17						STEP 18						STEP 19					
CONTENTS		G-BLL/R PRECHARGE						MEMORY DISCHARGE (VRW2)						SL SENSE						G-BLL/R DISCHARGE						DATA TRANSFER (SL(L) →G-BLL) G-BLR PRECHARGE						OPERATION (DLL, G-BLL)					
STATE OF MEMORY CELL	WRITE DATA	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR
01	11	1(0)	1	0	0	1.0	0(1)	1(0)	1	0	0	1.0	0(1)	1(0)	0	0	1	1	0(1)	1(0)	0.0	0	1	0.0	0(1)	1(0)	0.0	0	1	0.0	0(1)	1(0)	0.0	0	1	0.0	0(1)
00	11	1(0)	1	0	0	1.0	1(0)	1(0)	1	0	0	1.0	1(0)	1(0)	0	0	1	1	1(0)	1(0)	0.0	0	1	0.0	1(0)	1(0)	0.0	0	1	0.0	1(0)	1(0)	0.0	0	1	0.0	1(0)
10	11	1(0)	1	0	0	1.0	1(0)	1(0)	1	0	0	0.0	1(0)	1(0)	1	1	0	0	1(0)	1(0)	0.0	1	0	0.0	1(0)	1(0)	1.0	1	0	0.0	1(0)	1(0)	1.0	1	0	0.0	1(0)
11	01	0(1)	1	0	0	1.0	0(1)	0(1)	1	0	0	0.0	0(1)	0(1)	1	1	0	0	0(1)	0(1)	0.0	1	0	0.0	0(1)	0(1)	1.0	1	0	0.0	0(1)	0(1)	0.0	1	0	0.0	0(1)
	00	0(1)	1	0	0	1.0	1(0)	0(1)	1	0	0	0.0	1(0)	0(1)	1	1	0	0	1(0)	0(1)	0.0	1	0	0.0	1(0)	0(1)	1.0	1	0	0.0	1(0)	0(1)	0.0	1	0	0.0	1(0)
	10	1(0)	1	0	0	1.0	1(0)	1(0)	1	0	0	0.0	1(0)	1(0)	1	1	0	0	1(0)	1(0)	0.0	1	0	0.0	1(0)	1(0)	1.0	1	0	0.0	1(0)	1(0)	1.0	1	0	0.0	1(0)
	11	1(0)	1	0	0	1.0	0(1)	1(0)	1	0	0	0.0	0(1)	1(0)	1	1	0	0	0(1)	1(0)	0.0	1	0	0.0	0(1)	1(0)	1.0	1	0	0.0	0(1)	1(0)	1.0	1	0	0.0	0(1)

(b)

																		ERASE BACK						WRITE					
STEP 20						STEP 21						STEP 22						STEP 23						TO NORMAL WRITE STEP 2					
SL CLEAR DLL CLEAR						DL SENSE						G-BLL/R DISCHARGE						ERASE											
DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR
0	0.0	0	0	0.0	0(1)	(1)0	0.0	0	0	0.0	0(1)	(1)0	0.0	0	0	0.0	0(1)	(1)0					(0)1	(1)0					(0)1
0	0.0	0	0	0.0	1(0)	(1)0	0.0	0	0	0.0	1(0)	(1)0	0.0	0	0	0.0	1(0)	(1)0					(1)0	(1)0					(1)0
0	1.0	0	0	0.0	1(0)	(0)1	1.0	0	0	0.0	1(0)	(0)1	0.0	0	0	0.0	1(0)	(0)1					(1)0	(0)1					(1)0
0	0.0	0	0	0.0	0(1)	(1)0	0.0	0	0	0.0	0(1)	(1)0	0.0	0	0	0.0	0(1)	(1)0					(0)1	(1)0					(0)1
0	0.0	0	0	0.0	1(0)	(1)0	0.0	0	0	0.0	1(0)	(1)0	0.0	0	0	0.0	1(0)	(1)0					(1)0	(1)0					(1)0
0	1.0	0	0	0.0	1(0)	(0)1	1.0	0	0	0.0	1(0)	(0)1	0.0	0	0	0.0	1(0)	(0)1					(1)0	(0)1					(1)0
0	1.0	0	0	0.0	0(1)	(0)1	1.0	0	0	0.0	0(1)	(0)1	0.0	0	0	0.0	0(1)	(0)1					(0)1	(0)1					(0)1

FIG. 35

2. ERASE SEQUENCE

STEP	ERASE VERIFY 1																							
	STEP 1						STEP 2						STEP 3						STEP 4					
CONTENTS	G-BLL/R PRECHARGE						MEMORY DISCHARGE (VEV=2.0V)						SL SENSE & ALL DETERMINATION						G-BLL/R DISCHARGE, SL CLEAR					
	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR
11		0.5			1.0			0.5			1.0			0	0	1	1			0	0	0	0	
BELOW 11		0.5			1.0			0.5			1.0			0	0	1	1			0	0	0	0	

※ 11: BIT IN WHICH POST-ERASURE Vth IS LESS THAN OR EQUAL TO VEV

BELOW 11: BIT IN WHICH Vth OUT OF 11 IS LESS THAN OR EQUAL TO VWV0 (BIT INTENDED FOR WRITEBACK)

ALL DETERMINATION: ERASE END UPON PASS

ERASE						ERASE VERIFY 2																	
Step 5						Step 6						Step 7						Step 8					
ERASE						G-BLL/R PRECHARGE						MEMORY DISCHARGE (VEV=2.0V)						SL SENSE & ALL DETERMINATION					
DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR
							0.5			1.0			0.5			0.0			1	1	0	0	
							0.5			1.0			0.5			0.0			1	1	0	0	

ALL DETERMINATION: TO STEP 5 UPON FAIL

						'11' ERRATIC DETECTION																	
Step 9						Step 10						Step 11						Step 12					
G-BLL/R DISCHARGE, SL CLEAR						G-BLL/R PRECHARGE						MEMORY DISCHARGE (VWV0=1.2V)						SL SENSE & ALL DETERMINATION					
DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR
	0	0	0	0			0.5			1.0			0.5			1.0			0	0	1	1	
	0	0	0	0			0.5			1.0			0.5			0.0			1	1	0	0	

(a)

ALL DETERMINATION: ERASE END UPON PASS

WRITE (DEPLETE PREVENTING PROCESS)																							
Step 13						Step 14						Step 15						Step 16					
WRITE						G-BLL/R DISCHARGE G-BLL/R PRECHARGE						MEMORY DISCHARGE (VWV0=1.2V)						SL CLEAR, SL SENSE & ALL DETERMINATION					
DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR
	0.0	0.0	6.0	6.0			0.5	0	1	1.0			0.5	0	1	1.0			0	0	1	1	
	6.0	6.0	0.0	0.0			0.5	1	0	1.0			0.5	1	0	1.0			0	0	1	1	

ALL DETERMINATION: TO STEP 13 UPON FAIL

'11' ERRATIC DETECTION																							
Step 17						Step 18						Step 19						Step 20					
G-BLL/R PRECHARGE						MEMORY DISCHARGE (VWDS)						SL SENSE & ALL DETERMINATION						G-BLL/R DISCHARGE, SL CLEAR					
DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR	DLL	G-BLL	SL(L)	SL(R)	G-BLR	DLR
	0.5			1.0			0.5			0.0			1	1	0	0			0	0	0	0	
	0.5			1.0			0.5			0.0			1	1	0	0			0	0	0	0	

ALL DETERMINATION: ERASE END UPON PASS

FIG. 36

ADDITIONAL WRITE (LOGIC COMBINING PROCESS) OPERATING WAVEFORM

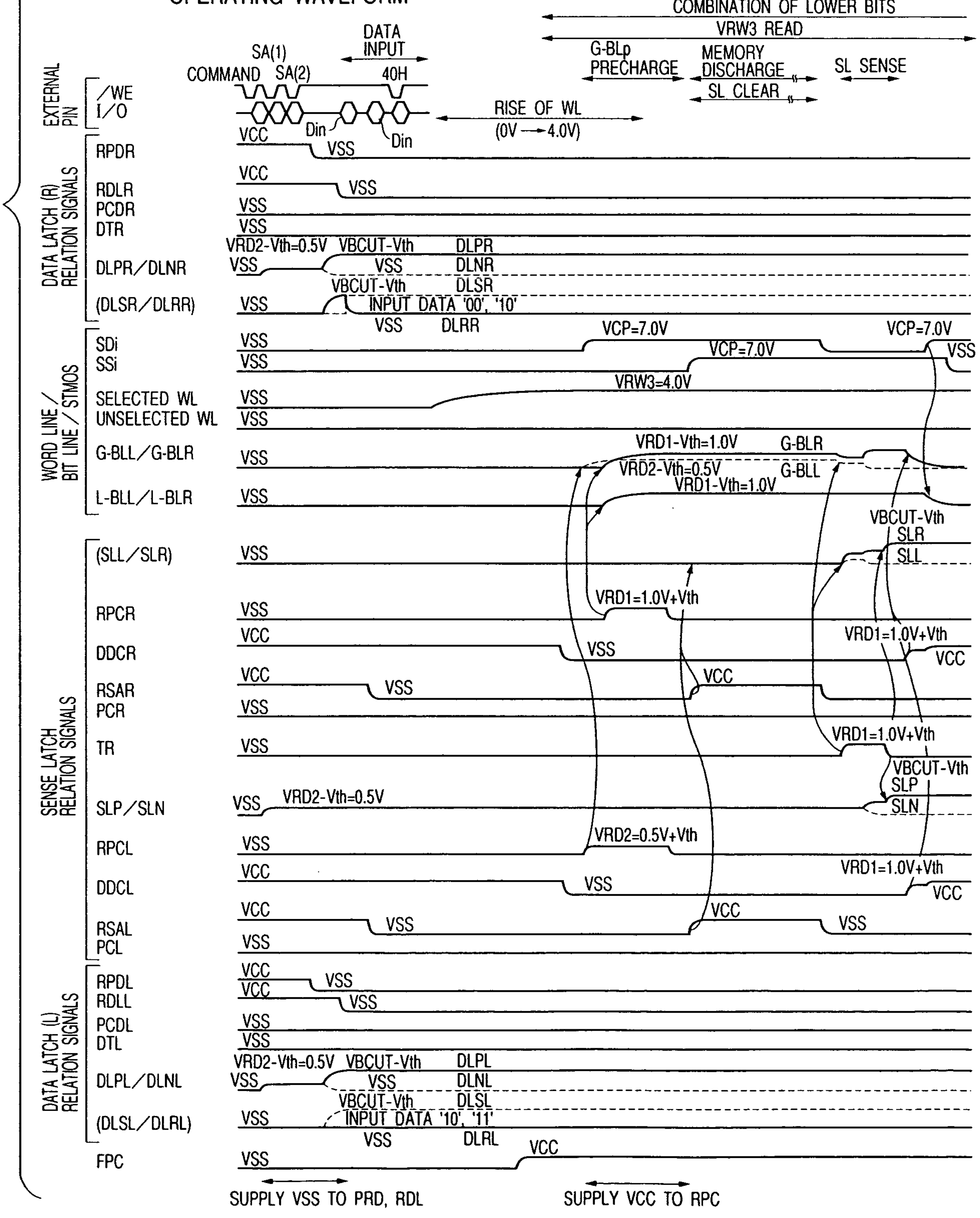
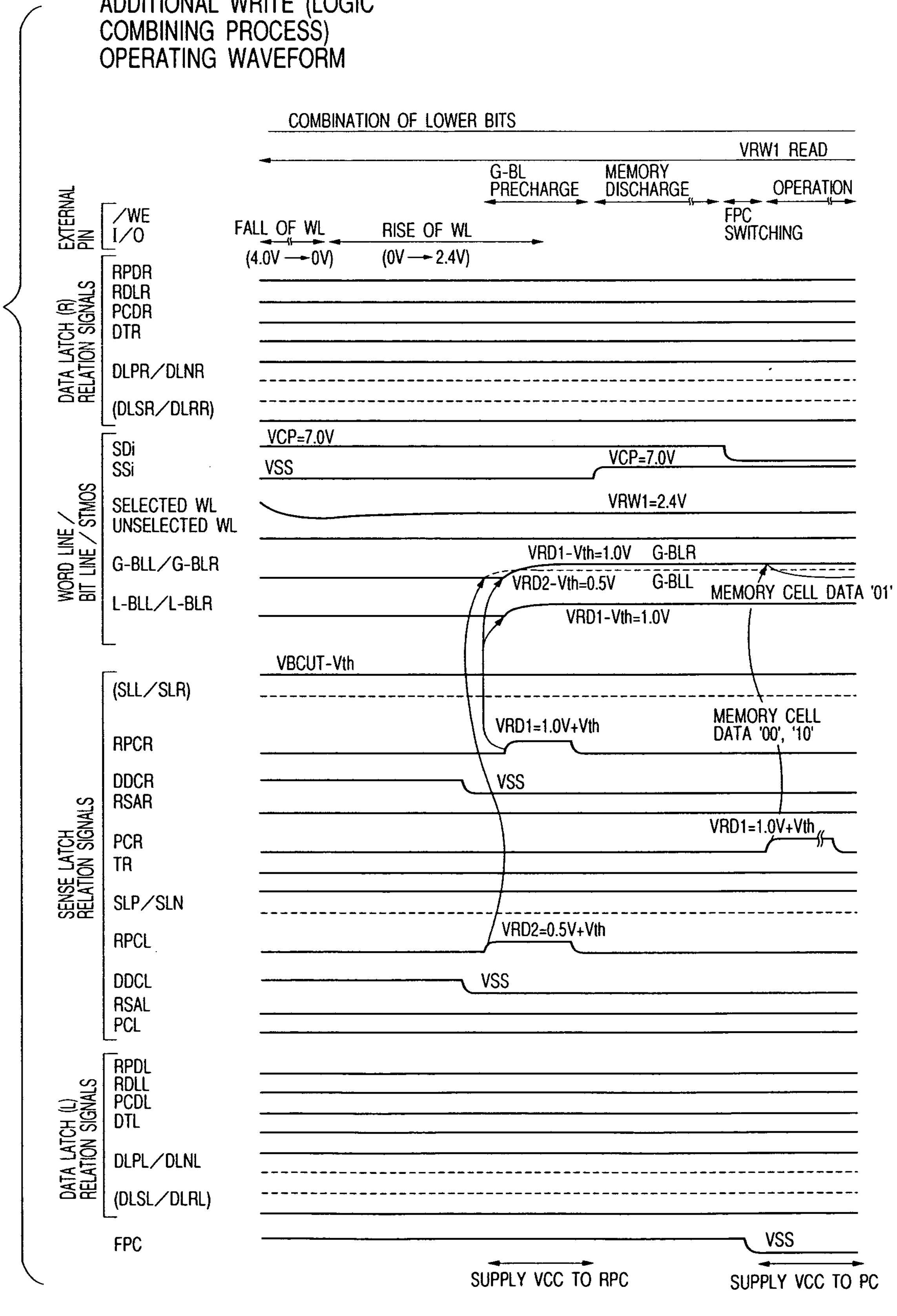


FIG. 37



ADDITIONAL WRITE (LOGIC COMBINING PROCESS) OPERATING WAVEFORM

FIG. 38

ADDITIONAL WRITE (LOGIC COMBINING PROCESS) OPERATING WAVEFORM

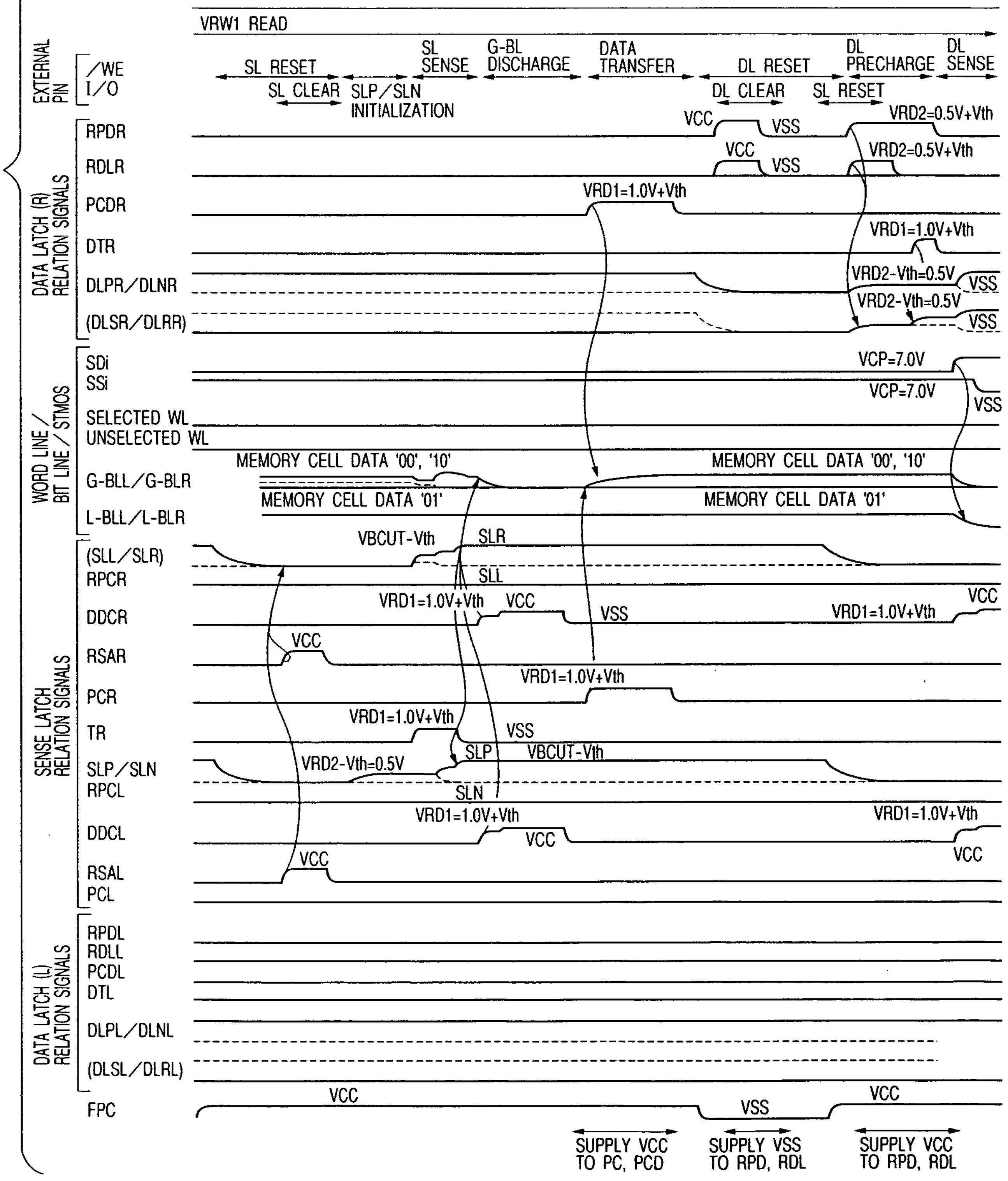


FIG. 39

ADDITIONAL WRITE (LOGIC COMBINING PROCESS) OPERATING WAVEFORM

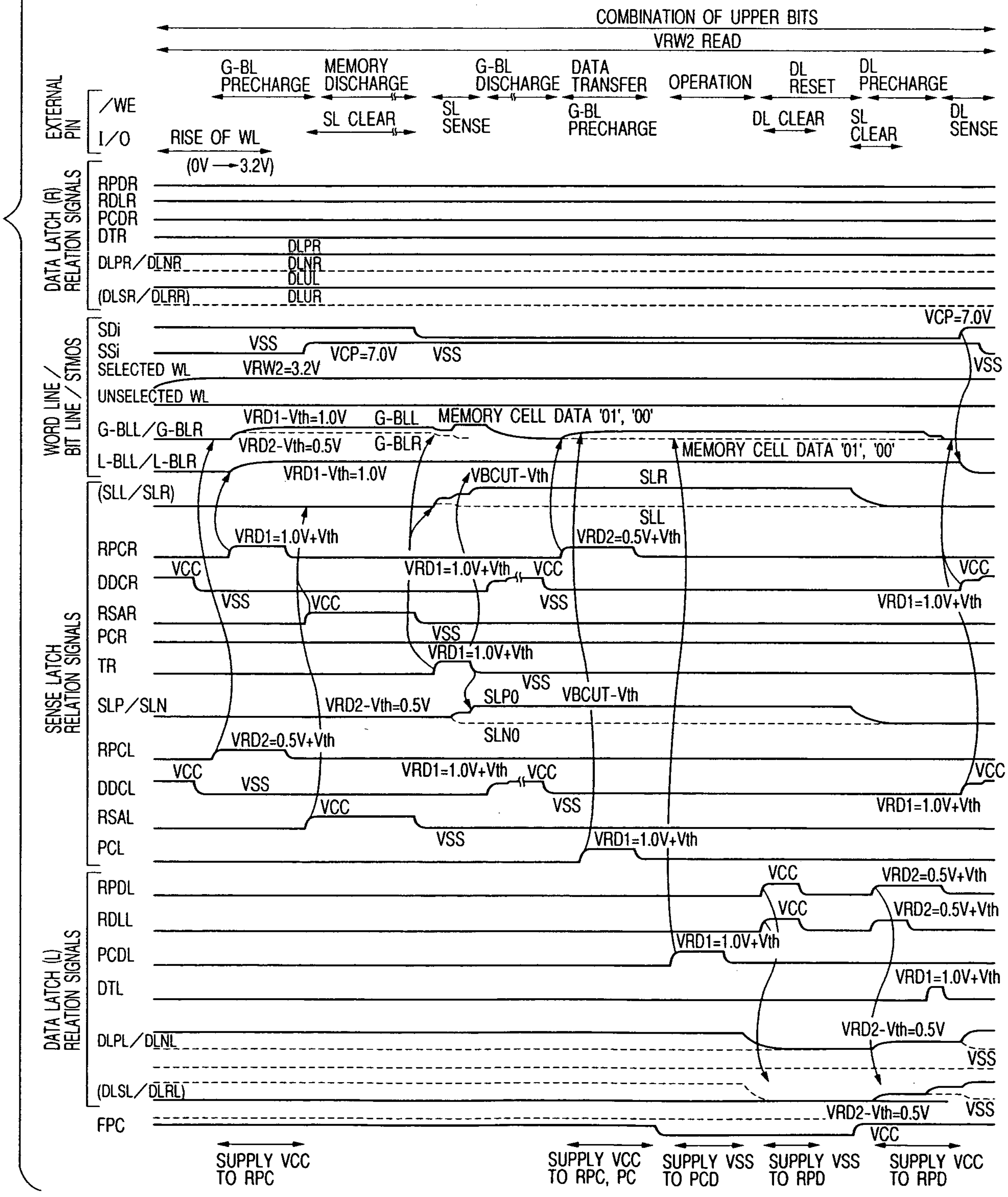


FIG. 40

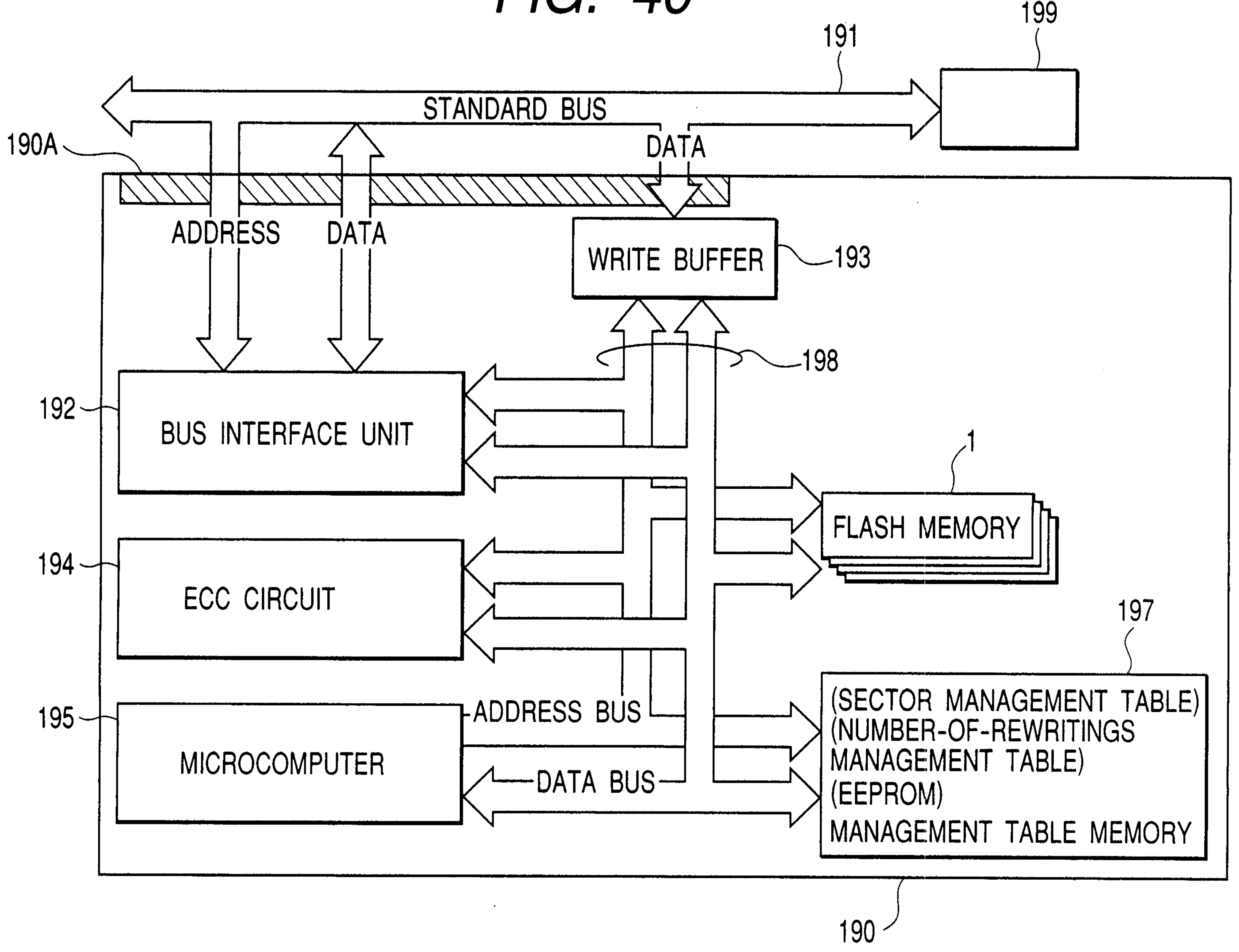
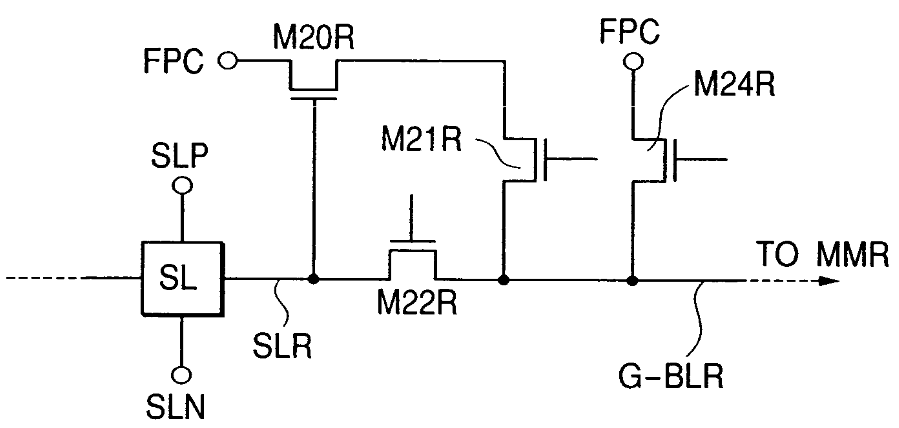

199
191
STANDARD BUS
DATA
190A
ADDRESS
DATA
WRITE BUFFER
193
198
192
BUS INTERFACE UNIT
1
FLASH MEMORY
194
ECC CIRCUIT
197
195
MICROCOMPUTER
ADDRESS BUS
DATA BUS
(SECTOR MANAGEMENT TABLE)
(NUMBER-OF-REWRITINGS
MANAGEMENT TABLE)
(EEPROM)
MANAGEMENT TABLE MEMORY
190

FIG. 41



PRECHARGE
- OPERATION UNSELECT MAT ⟶ G-BLL=0.5V (VIA M24L)
- OPERATION SELECT MAT ⟶ G-BLR=1V (VIA M24R)

WRITE VERIFY
- WRITE COMPLETION : G-BLR=1V
- WRITE UNCOMPLETION : G-BLR=0V (DISCHARGE VIA MC)

MASK PRECHARGE
- SLR=0 : WRITE SELECT
- SLR=1 : WRITE UNSELECT ⟶ G-BLR=1V (PRECHARGE VIA M20R, M21R)

LATCH
- SLR=0 : WRITE UNCOMPLETION
- SLR=1 : WRITE COMPLETION

FIG. 42

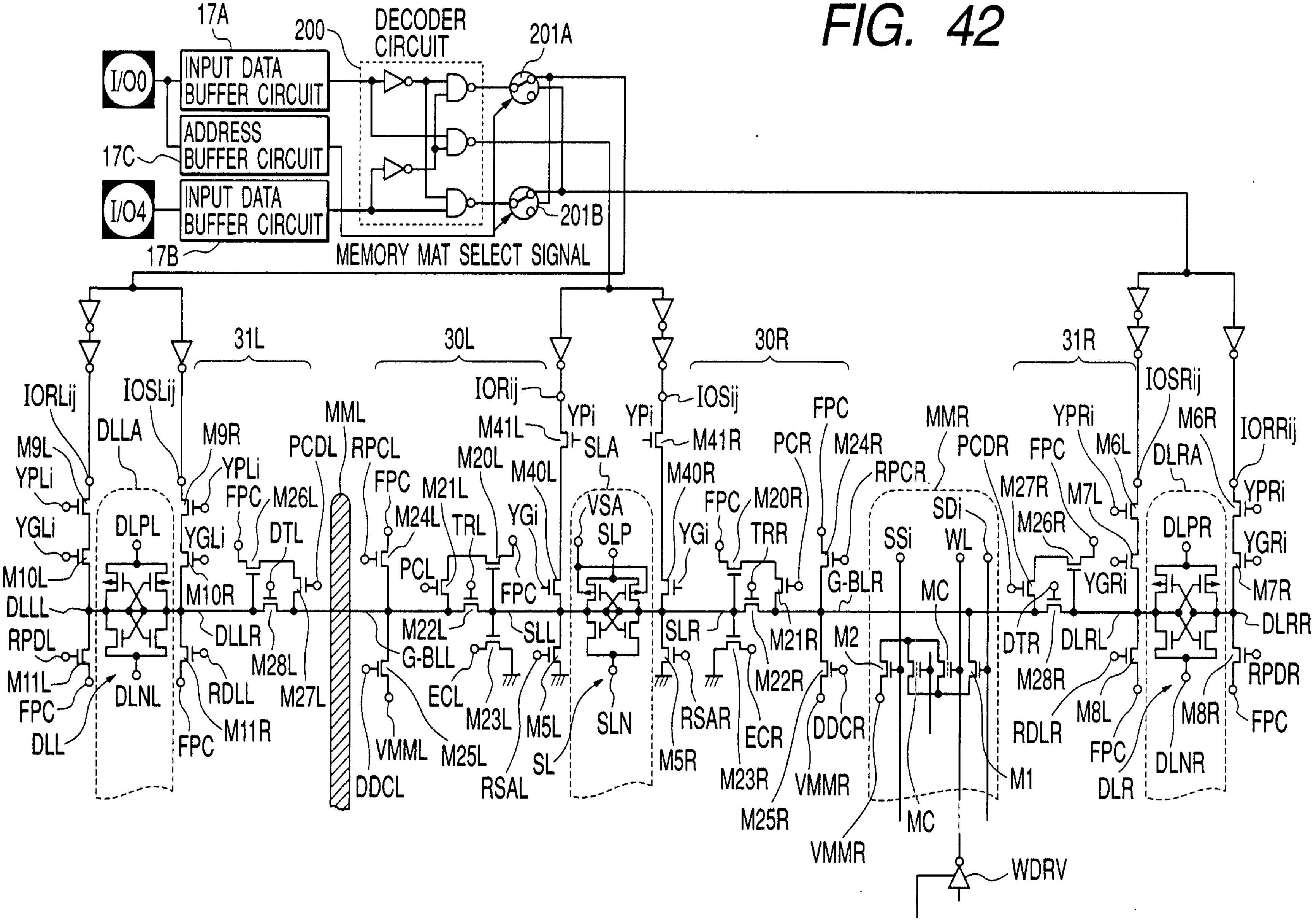

17A
200
DECODER CIRCUIT
201A
I/O0
INPUT DATA BUFFER CIRCUIT
ADDRESS BUFFER CIRCUIT
17C
I/O4
INPUT DATA BUFFER CIRCUIT
201B
17B
MEMORY MAT SELECT SIGNAL
31L
30L
30R
31R
IORLij
IOSLij
DLLA
M9R
M9L
YPLi
YPLi
FPC
M26L
DTL
MML
PCDL
RPCL
FPC
M24L
M21L
M20L
M40L
IORij
M41L
YPi
SLA
YPi
IOSij
M41R
M40R
FPC
M20R
TRR
PCR
FPC
M24R
RPCR
MMR
PCDR
FPC
YPRi
M6L
IOSRij
M6R
DLRA
IORRij
YGLi
DLPL
YGLi
TRL
YGi
VSA
SLP
YGi
SDi
SSi
WL
M27R
M26R
M7L
DLPR
YPRi
YGRi
M10L
DLLL
M10R
PCL
FPC
G-BLR
MC
YGRi
M7R
DLRR
RPDL
DLLR
M22L
SLL
SLR
M21R
M2
DTR
DLRL
M28L
G-BLL
M22R
M28R
RPDR
M11L
FPC
DLL
DLNL
RDLL
FPC
M11R
M27L
ECL
M23L
M5L
SL
SLN
RSAR
ECR
DDCR
RDLR
M8L
M8R
FPC
DDCL
VMML
M25L
RSAL
M5R
M23R
VMMR
M1
FPC
DLR
DLNR
M25R
MC
VMMR
WDRV

FIG. 43

SL/DL CIRCUIT LATCH DATA

WRITE DATA	UPPER DATA I/O4	LOWER DATA I/O0	UPON SELECTION OF LEFT MAT			UPON SELECTION OF RIGHT MAT		
			DLL	SL	DLR	DLL	SL	DLR
"01"	0	1	1	0	1	1	0	1
"00"	0	0	1	1	0	0	1	1
"10"	1	0	0	1	1	1	1	0
"11"	1	1	1	1	1	1	1	1

FIG. 44

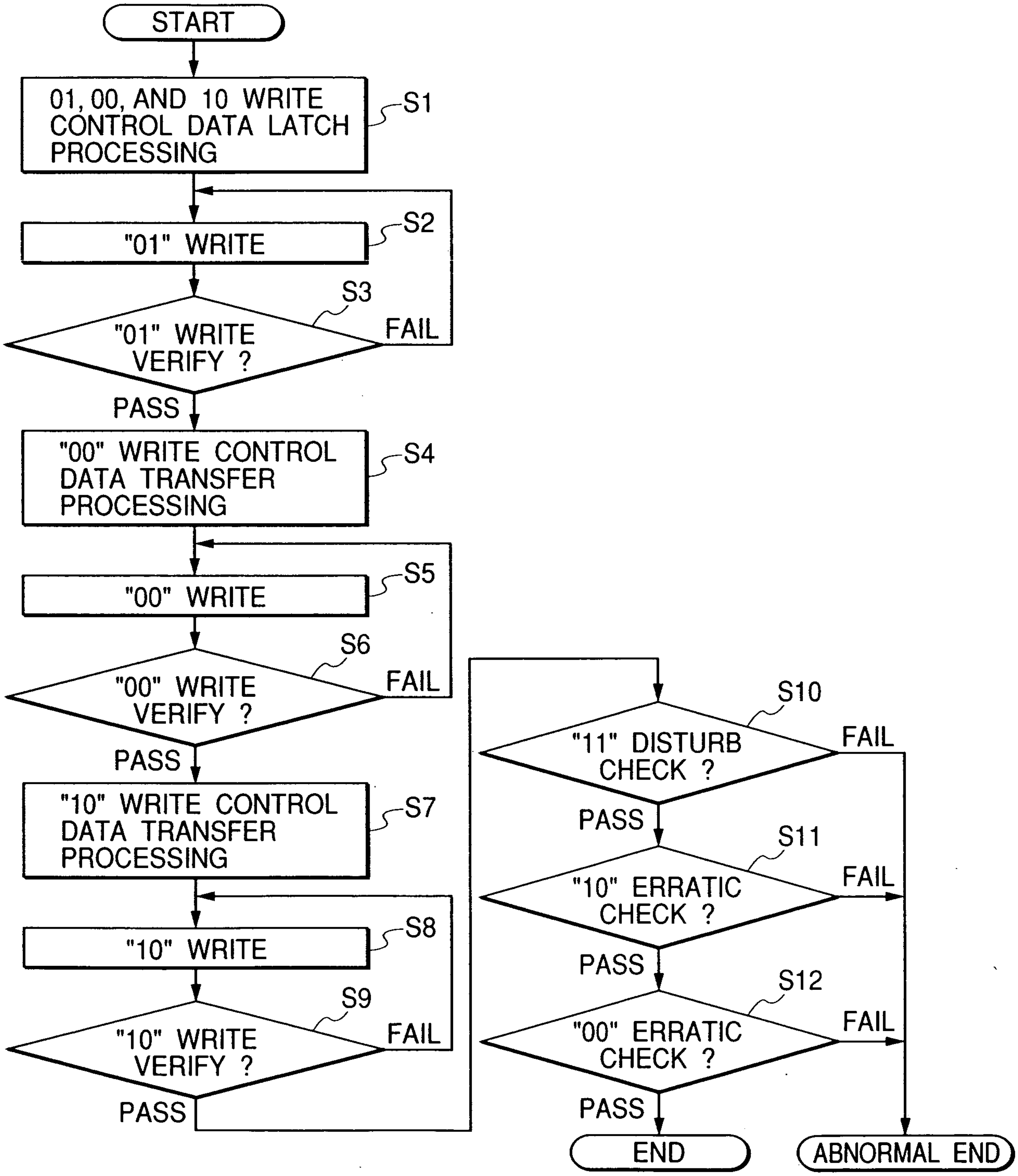

START
01, 00, AND 10 WRITE CONTROL DATA LATCH PROCESSING
S1
"01" WRITE
S2
"01" WRITE VERIFY ?
S3
FAIL
PASS
"00" WRITE CONTROL DATA TRANSFER PROCESSING
S4
"00" WRITE
S5
"00" WRITE VERIFY ?
S6
FAIL
PASS
"10" WRITE CONTROL DATA TRANSFER PROCESSING
S7
"10" WRITE
S8
"10" WRITE VERIFY ?
S9
FAIL
PASS
"11" DISTURB CHECK ?
S10
FAIL
PASS
"10" ERRATIC CHECK ?
S11
FAIL
PASS
"00" ERRATIC CHECK ?
S12
FAIL
PASS
END
ABNORMAL END

FIG. 45

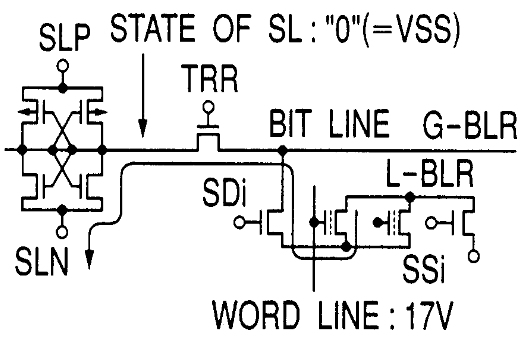
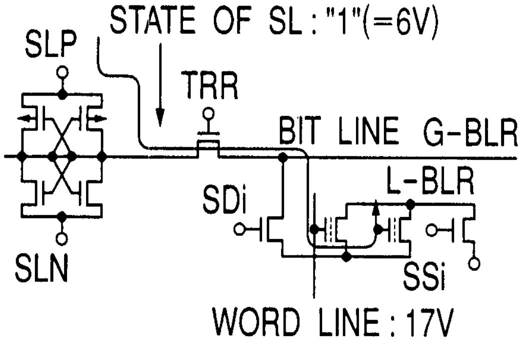
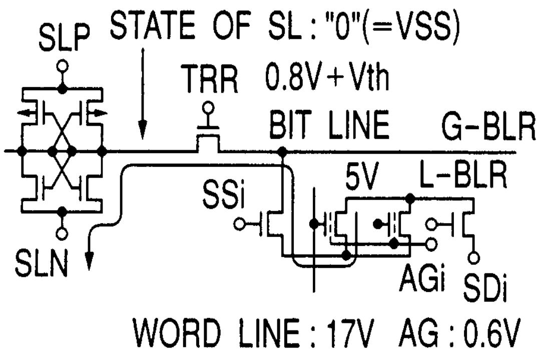
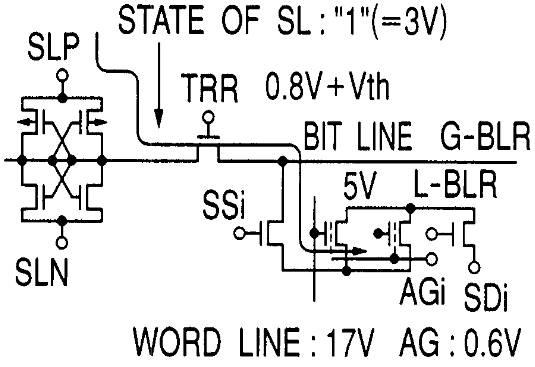
	WRITE SELECT (SL="0")	WRITE UNSELECT (SL="1")
AND MEMORY CELL	 SLP STATE OF SL : "0"(=VSS) TRR BIT LINE G-BLR L-BLR SDi SLN SSi WORD LINE : 17V MEMORY CELL : Vcg=17V → FN TUNNEL WRITING	 SLP STATE OF SL : "1"(=6V) TRR BIT LINE G-BLR L-BLR SDi SLN SSi WORD LINE : 17V MEMORY CELL : Vcg=11V → WRITE UNSELECTION
AG-AND MEMORY CELL	 SLP STATE OF SL : "0"(=VSS) TRR 0.8V+Vth BIT LINE G-BLR 5V L-BLR SSi SLN AGi SDi WORD LINE : 17V AG : 0.6V MEMORY CELL : Vds=5V → HC WRITE	 SLP STATE OF SL : "1"(=3V) TRR 0.8V+Vth BIT LINE G-BLR 5V L-BLR SSi SLN AGi SDi WORD LINE : 17V AG : 0.6V MEMORY CELL : Vds=0V (AG : CUT OFF) → WRITE UNSELECTION

FIG. 46

("11" DISTURB CHECK)

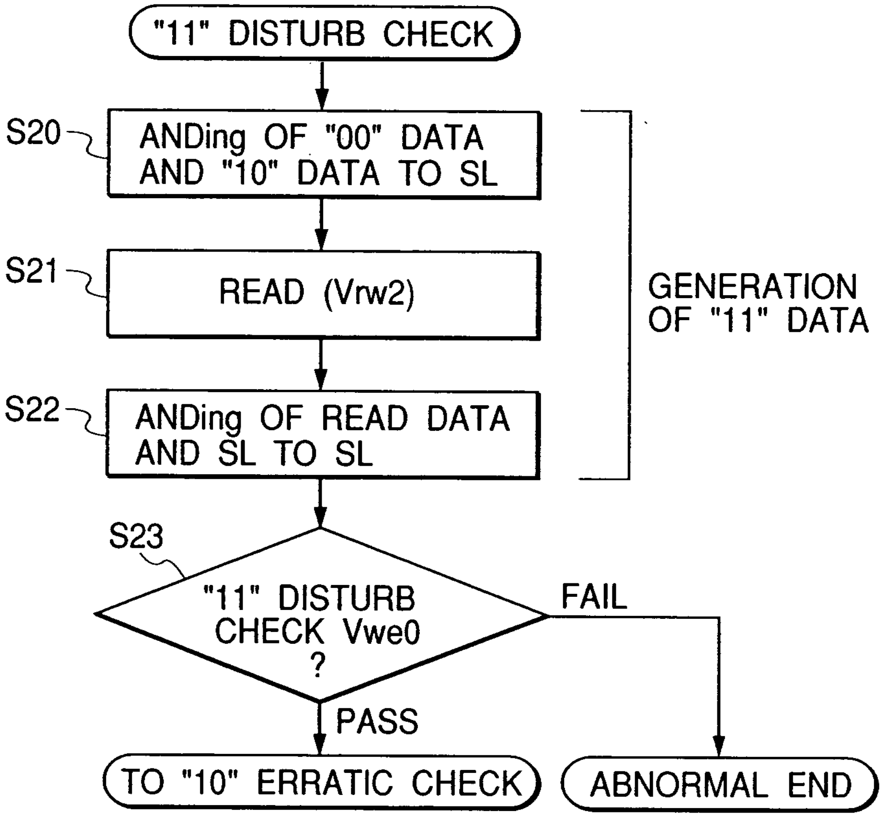


FIG. 47

(GENERATION OF "11" DATA)

<"01" HEMMING BOTTOM MEASURES>
READ READ WORD VOLTAGE AT Vrw2 RATHER THAN AT Vrw3

<MASK PROCESSING>
"00"/"10" MASK PROCESSING USE DATA IN DL CIRCUIT

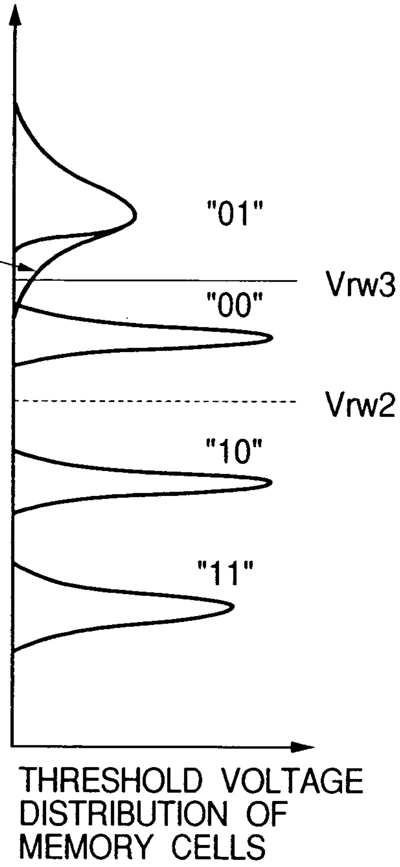


FIG. 48

(4) "11" DISTURB CHECK

WRITE DATA	"11" DISTURB CHECK																							
	STEP 30						STEP 31						STEP 32						STEP 33					
	SL CLEAR BL(L)/(R) CLEAR						BL(R) PRECHARGE BL(L) PRECHARGE						DL(R) SELECT DISCHARGE						SL SENSE					
	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)
"01"	0	0	0	0	0	1	0	0.5	0	0	1	1	0	0.5	0	0	0	1	0	1	1	0	0	1
"00"	1	0	0	0	0	1	1	0.5	0	0	1	1	1	0.5	0	0	0	1	1	1	1	0	0	1
"10"	0	0	0	0	0	0	0	0.5	0	0	1	0	0	0.5	0	0	1	0	0	0	0	1	1	0
"11"	0	0	0	0	0	1	0	0.5	0	0	1	1	0	0.5	0	0	0	1	0	1	1	0	0	1

WRITE DATA	STEP 34						STEP 35						STEP 36						STEP 37					
	DL(L) SELECT DISCHARGE BL(R) DISCHARGE						BL(R) PRECHARGE						SL CLEAR SL SENSE						BL(L)/(R) DISCHARGE					
	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)
"01"	0	1	1	0	0	1	0	1	1	0	0.5	1	0	1	1	0	0	1	0	0	1	0	0	1
"00"	1	0	1	0	0	1	1	0	1	0	0.5	1	1	0	0	1	1	1	1	0	0	1	0	1
"10"	0	0	0	1	0	0	0	0	0	1	0.5	0	0	0	0	1	1	0	0	0	0	1	0	0
"11"	0	1	1	0	0	1	0	1	1	0	0.5	1	0	1	1	0	0	1	0	0	1	0	0	1

WRITE DATA	STEP 38						STEP 39						STEP 40						STEP 41					
	BL(L)/(R) PRECHARGE						MEMORY DISCHARGE (Vrw2)						BL(R) SELECT PRECHARGE						SL SENSE					
	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)
"01"	0	0.5	1	0	1	1	0	0.5	1	0	1	1	0	0.5	1	0	1	1	0	0	0	1	1	1
"00"	1	0.5	0	1	1	1	1	0.5	0	1	1	1	1	0.5	0	1	1	1	1	0	0	1	1	1
"10"	0	0.5	0	1	1	0	0	0.5	0	1	0	0	0	0.5	0	1	1	0	0	0	0	1	1	0
"11"	0	0.5	1	0	1	1	0	0.5	1	0	0	1	0	0.5	1	0	0	1	0	1	1	0	0	1

WRITE DATA	STEP 42						STEP 43						STEP 44						STEP 45					
	BL(L)/(R) DISCHARGE BL(L)/(R) PRECHARGE						BL(R) SELECT DISCHARGE						MEMORY DISCHARGE (Vwe0)						SL SENSE ALL DETERMINATION					
	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)
"01"	0	0.5	0	1	1	1	0	0.5	0	1	0	1	0	0.5	0	1	0	1	0	1	1	0	0	1
"00"	1	0.5	0	1	1	1	1	0.5	0	1	0	1	1	0.5	0	1	0	1	1	1	1	0	0	1
"10"	0	0.5	0	1	1	0	0	0.5	0	1	0	0	0	0.5	0	1	0	0	0	1	1	0	0	0
"11"	0	0.5	1	0	1	1	0	0.5	1	0	1	1	0	0.5	1	0	0	1	0	1	1	0	0	1

▲ IN THE CASE OF PASS

FIG. 49

(RESTORATION OF "01" DATA)

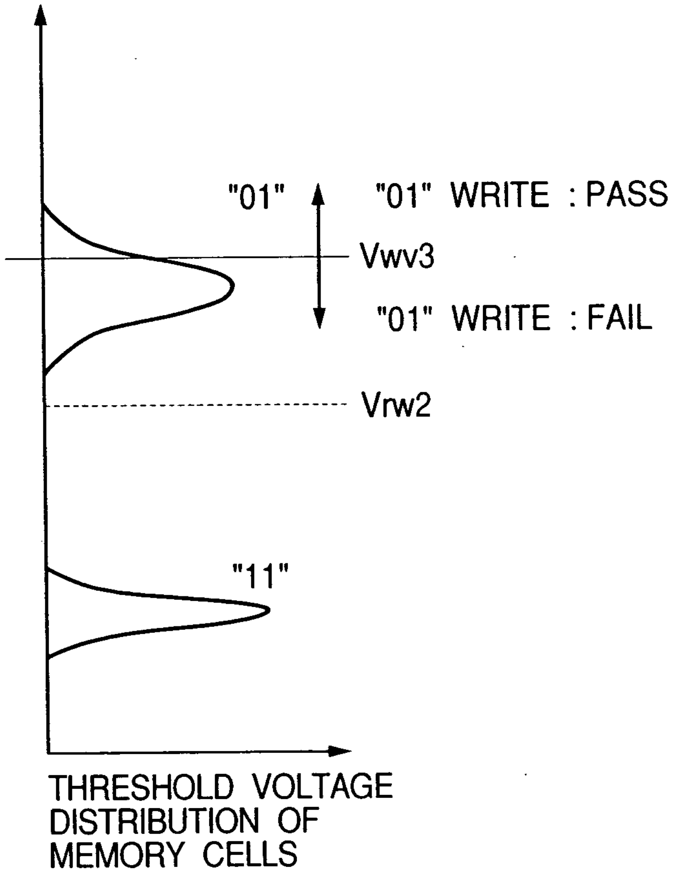
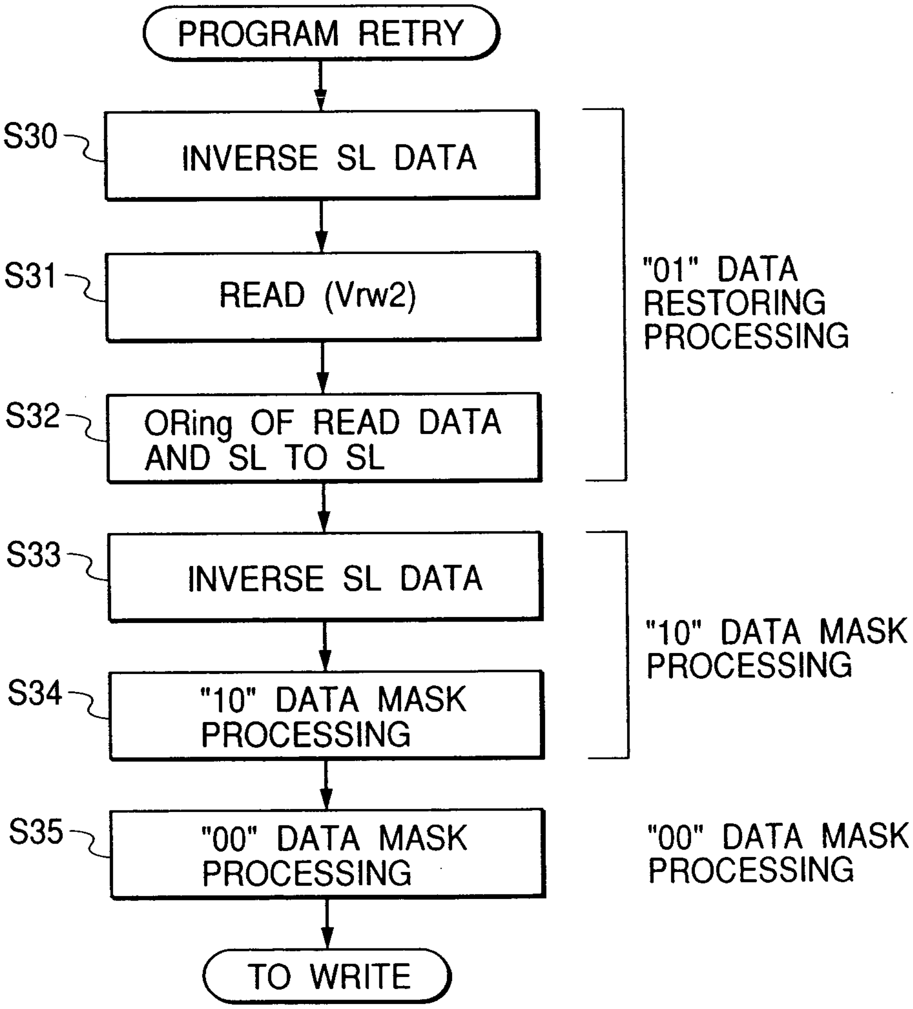


FIG. 50

(PROGRAM RETRY)


PROGRAM RETRY
S30
INVERSE SL DATA
S31
READ (Vrw2)
S32
ORing OF READ DATA AND SL TO SL
"01" DATA RESTORING PROCESSING
S33
INVERSE SL DATA
S34
"10" DATA MASK PROCESSING
"10" DATA MASK PROCESSING
S35
"00" DATA MASK PROCESSING
"00" DATA MASK PROCESSING
TO WRITE

(PROGRAM RETRY)
(1) DATA RESTORING PROCESSING

FIG. 51

WRITE DATA		INITIAL STATE						'01' DATA RESTORING PROCESSING + "11" DATA MASK PROCESSING																													
								SL INVERSION																													
		STEP 0						STEP 1						STEP 2						STEP 3						STEP 4											
		STATE OF ON-"01" WRITE ABNORMAL COMPLETION						BL(L)／(R) PRECHARGE						SELECT DISCHARGE SL(R)						SL CLEAR SL SENSE						BL(L)／(R) DISCHARGE											
		DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)						
"01"	FAIL	0		1	0		1	0	0.4	1	0	0.7	1	0	0.4	1	0	0.7	1	0	0	0	1	0.7	1	0	0	0	1	0	1						
	PASS	0		0	1		1	0	0.4	0	1	0.7	1	0	0.4	0	1	0	1	0	0.7	1	0	0	1	0	0	1	0	0	1						
"00"		1		0	1		1	1	0.4	0	1	0.7	1	1	0.4	0	1	0	1	1	0.7	1	0	0	1	1	0	1	0	0	1						
"10"		0		0	1		0	0	0.4	0	1	0.7	0	0	0.4	0	1	0	0	0	0.7	1	0	0	0	0	0	1	0	0	0						
"11"		0		0	1		1	0	0.4	0	1	0.7	1	0	0.4	0	1	0	1	0	0.7	1	0	0	1	0	0	1	0	0	1						

▲ GUARANTEE ONLY DL IN INITIAL STAGE

"11" DATA MASK PROCESSING																													
STEP 5						STEP 6						STEP 7						STEP 8						STEP 9					
BL(L)／(R) PRECHARGE						MEMORY DISCHARGE Vrw2						SELECT PRECHARGE SL(R)						SL CLEAR SL SENSE						BL(L)／(R) DISCHARGE					
DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)
0	0.4	0	1	0.7	1	0	0.4	0	1	0.7/0	1	0	0.4	0	1	0.7	1	0	0	0	1	0.7	1	0	0	0	1	0	1
0	0.4	1	0	0.7	1	0	0.4	1	0	0.7	1	0	0.4	1	0	0.7	1	0	0	0	1	0.7	1	0	0	0	1	0	1
1	0.4	1	0	0.7	1	1	0.4	1	0	0	1	1	0.4	1	0	0	1	1	0.7	1	0	0	1	1	0	1	0	0	1
0	0.4	1	0	0.7	0	0	0.4	1	0	0	0	0	0.4	1	0	0	0	0	0.7	1	0	0	0	0	0	1	0	0	0
0	0.4	1	0	0.7	1	0	0.4	1	0	0	1	0	0.4	1	0	0	1	0	0.7	1	0	0	1	0	0	1	0	0	1

▲ "01" FAIL MEANS THAT Vth STATE IS DIVIDED WITH Vrw2 AS BORDER
▲ MASK "01" FAIL

FIG. 52

WRITE DATA	"10" DATA MASK PROCESSING																							
	SL INVERSION																							
	STEP 10						STEP 11						STEP 12						STEP 13					
	BL(L)/(R) PRECHARGE						BL(R) SELECT DISCHARGE						SL CLEAR SL SENSE						BL(L)/(R) DISCHARGE					
	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)
"01" FAIL	0	0.4	0	1	0.7	1	0	0.4	0	1	0	1	0	0.7	1	0	0	1	0	0	1	0	0	1
"01" PASS	0	0.4	0	1	0.7	1	0	0.4	0	1	0	1	0	0.7	1	0	0	1	0	0	1	0	0	1
"00"	1	0.4	0/1	1/0	0.7	1	1	0.4	0/1	1/0	0/0.7	1	1	0.7/0	1/0	0/1	0/0.7	1	1	0	1/0	0/1	0	1
"10"	0	0.4	0/1	1/0	0.7	0	0	0.4	0/1	1/0	0/0.7	0	0	0.7/0	1/0	0/1	0/0.7	0	0	0	1/0	0/1	0	0
"11"	0	0.4	1	0	0.7	1	0	0.4	1	0	0.7	1	0	0	0	1	0.7	1	0	0	0	1	0	1

▲ VALUE OF SL VARIES ACCORDING TO Vth STATE UPON "00" AND "10" WRITE ABNORMAL END AFTER STEP 10, DESCRIBE "00" AND "10" ABNORMAL END IN CONSIDERATION THEREOF

"10" DATA MASK PROCESSING																							
STEP 14						STEP 15						STEP 16						STEP 17					
BL(L)/(R) PRECHARGE						BL(R) SELECT DISCHARGE DL(R)						BL(R) SELECT PRECHARGE SL(R)						SL CLEAR SL SENSE					
DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)
0	0.4	1	0	0.7	1	0	0.4	1	0	0	1	0	0.4	1	0	0	1	0	0.7	1	0	0	1
0	0.4	1	0	0.7	1	0	0.4	1	0	0	1	0	0.4	1	0	0	1	0	0.7	1	0	0	1
1	0.4	1/0	0/1	0.7	1	1	0.4	1/0	0/1	0	1	1	0.4	1/0	0/1	0/0.7	1	1	0.7/0	1/0	0/1	0/0.7	1
0	0.4	1/0	0/1	0.7	0	0	0.4	1/0	0/1	0.7	0	0	0.4	1/0	0/1	0.7	0	0	0	0	1	0.7	0
0	0.4	0	1	0.7	1	0	0.4	0	1	0	1	0	0.4	0	1	0.7	1	0	0	0	1	0.7	1

"00" DATA MASK PROCESSING																	
STEP 18						STEP 19						STEP 20					
BL(L) SELECT DISCHARGE BL(R) DISCHARGE						BL(R) PRECHARGE						SL CLEAR SL SENSE					
DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)
0	0.7	1	0	0	1	0	0.7	1	0	0.4	1	0	0.7	1	0	0	1
0	0.7	1	0	0	1	0	0.7	1	0	0.4	1	0	0.7	1	0	0	1
1	0	1/0	0/1	0	1	1	0	1/0	0/1	0.4	1	1	0	0	1	0.7	1
0	0	0	1	0	0	0	0	0	1	0.4	0	0	0	0	1	0.7	0
0	0	0	1	0	1	0	0	0	1	0.4	1	0	0	0	1	0.7	1

FIG. 53

(DATA RECOVERY READ)

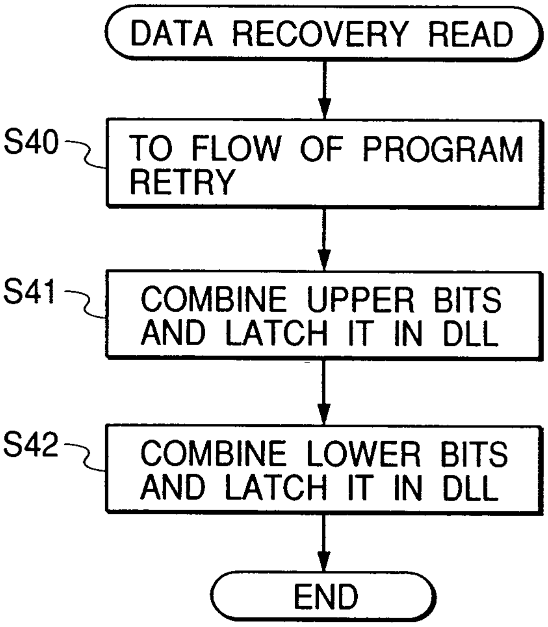

DATA RECOVERY READ
S40
TO FLOW OF PROGRAM RETRY
S41
COMBINE UPPER BITS AND LATCH IT IN DLL
S42
COMBINE LOWER BITS AND LATCH IT IN DLL
END

FIG. 54

(DATA RECOVERY READ)

WRITE DATA	DATA LATCH PROCESSING (COMBINATION OF UPPER BITS)																							
	STEP 0						STEP 1						STEP 2						STEP 3					
	INITIAL DATA						BL(L) PRECHARGE						BL(L) SELECT DISCHARGE DL(L)						BL(L) SELECT DISCHARGE SL(L)					
	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)
"01"	0		1	0		1	0	1.2	1	0		1	0	1.2	1	0		1	0	0	1	0		1
"00"	1		0	1		1	1	1.2	0	1		1	1	0	0	1		1	1	0	0	1		1
"10"	0		0	1		0	0	1.2	0	1		0	0	1.2	0	1		0	0	1.2	0	1		0
"11"	0		0	1		1	0	1.2	0	1		1	0	1.2	0	1		1	0	1.2	0	1		1

▲ AFTER COMPLETION OF PROGRAM RETRY DATA LATCH

STEP 4						STEP 5					
DL(L) CLEAR DL(L) SENSE						BL(L) DISCHARGE					
DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)
0	0	1	0		1	0	0	1	0		1
0	0	0	1		1	0	0	0	1		1
1	1.2	0	1		0	1	0	0	1		0
1	1.2	0	1		1	1	0	0	1		1

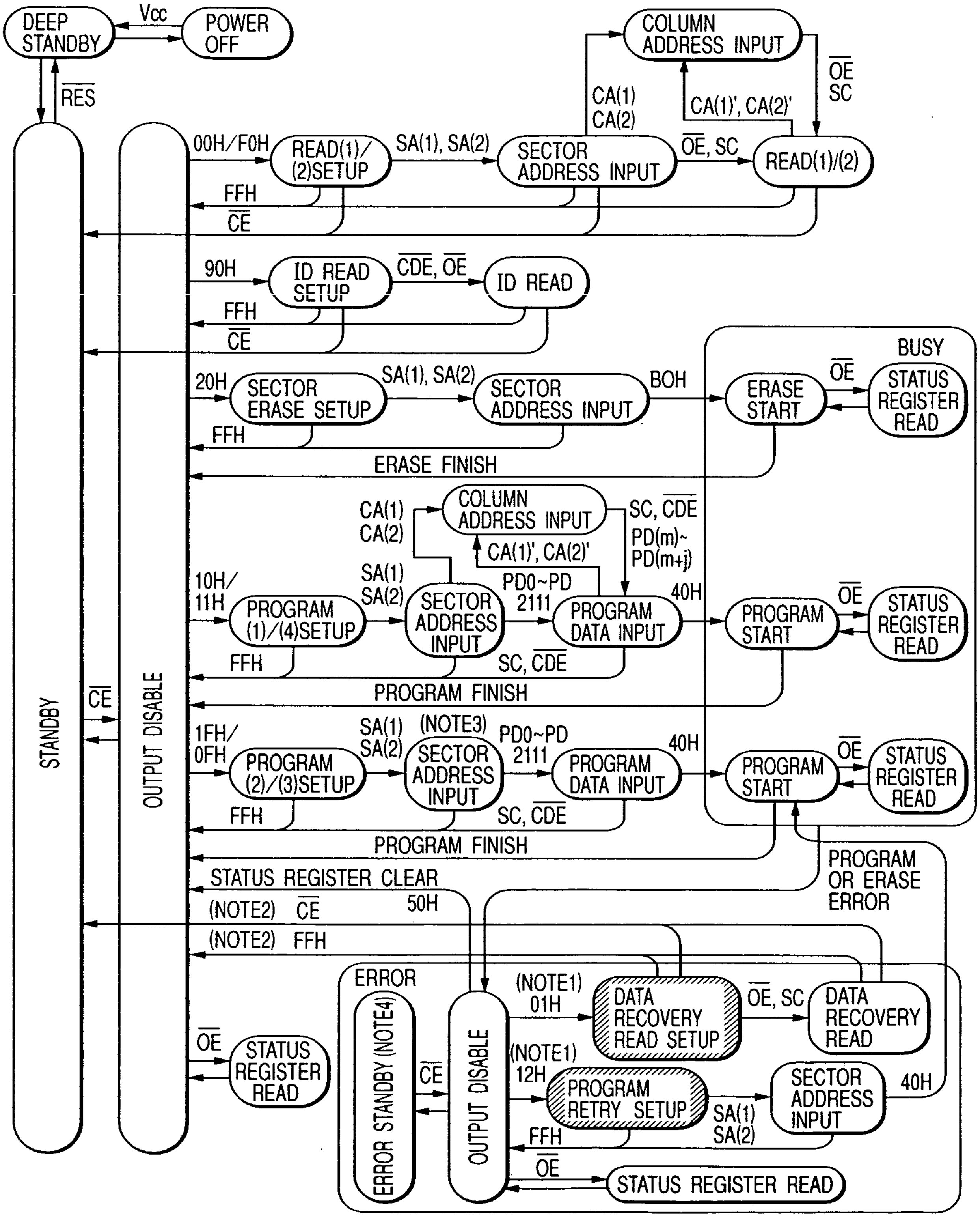
▲ DETERMINATION OF UPPER BIT

(COMBINATION OF LOWER BITS)																							
STEP 6						STEP 7						STEP 8						STEP 9					
BL(L) SELECT PRECHARGE DL(L) & SL(L)						BL(R) PRECHARGE						SL CLEAR SL SENSE						BL(L)/(R) DISCHARGE					
DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)
0	0.7	1	0		1	0	0.7	1	0	0.4	1	0	0.7	0.7	0	0	1	0	0	1	0	0	1
0	0	0	1		1	0	0	0	1	0.4	1	0	0	0	0.4	0.4	1	0	0	0	1	0	1
1	0.7	0	1		0	1	0.7	0	1	0.4	0	1	0.7	0.7	0	0	0	1	0	1	0	0	0
1	0.7	0	1		1	1	0.7	0	1	0.4	1	1	0.7	0.7	0	0	1	1	0	1	0	0	1

STEP 10						STEP 11						STEP 12						STEP 13					
BL(R) PRECHARGE						BL(R) SELECT DISCHARGE DL(R)						BL(R) SELECT PRECHARGE SL(R)						DL(R) CLEAR DL(R) SENSE					
DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)	DL(L)	BL(L)	SL(L)	SL(R)	BL(R)	DL(R)
0	0	1	0	1.2	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	0
0	0	0	1	1.2	1	0	0	0	1	0	1	0	0	0	1	1.2	1	0	0	0	1	1.2	1
1	0	1	0	1.2	0	1	0	1	0	1.2	0	1	0	1	0	1.2	0	1	0	1	0	1.2	1
1	0	1	0	1.2	1	1	0	1	0	0	1	1	0	1	0	0	1	1	0	1	0	0	0

▲
DETERMINATION OF LOWER BIT

FIG. 55


DEEP STANDBY
Vcc
POWER OFF
$\overline{RES}$
COLUMN ADDRESS INPUT
$\overline{OE}$
SC
CA(1)
CA(2)
CA(1)', CA(2)'
00H/F0H
READ(1)/(2)SETUP
SA(1), SA(2)
SECTOR ADDRESS INPUT
$\overline{OE}$, SC
READ(1)/(2)
FFH
$\overline{CE}$
90H
ID READ SETUP
$\overline{CDE}$, $\overline{OE}$
ID READ
FFH
$\overline{CE}$
BUSY
20H
SECTOR ERASE SETUP
SA(1), SA(2)
SECTOR ADDRESS INPUT
BOH
ERASE START
$\overline{OE}$
STATUS REGISTER READ
FFH
ERASE FINISH
CA(1)
CA(2)
COLUMN ADDRESS INPUT
SC, $\overline{CDE}$
PD(m)~
PD(m+j)
CA(1)', CA(2)'
10H/
11H
PROGRAM (1)/(4)SETUP
SA(1)
SA(2)
SECTOR ADDRESS INPUT
PD0~PD
2111
PROGRAM DATA INPUT
40H
PROGRAM START
$\overline{OE}$
STATUS REGISTER READ
FFH
SC, $\overline{CDE}$
PROGRAM FINISH
STANDBY
$\overline{CE}$
OUTPUT DISABLE
1FH/
0FH
PROGRAM (2)/(3)SETUP
SA(1)
SA(2)
(NOTE3)
SECTOR ADDRESS INPUT
PD0~PD
2111
PROGRAM DATA INPUT
40H
PROGRAM START
$\overline{OE}$
STATUS REGISTER READ
FFH
SC, $\overline{CDE}$
PROGRAM FINISH
STATUS REGISTER CLEAR
50H
PROGRAM OR ERASE ERROR
(NOTE2) $\overline{CE}$
(NOTE2) FFH
ERROR
(NOTE1)
01H
DATA RECOVERY READ SETUP
$\overline{OE}$, SC
DATA RECOVERY READ
$\overline{OE}$
STATUS REGISTER READ
ERROR STANDBY (NOTE4)
$\overline{CE}$
OUTPUT DISABLE
(NOTE1)
12H
PROGRAM RETRY SETUP
SA(1)
SA(2)
SECTOR ADDRESS INPUT
40H
FFH
$\overline{OE}$
STATUS REGISTER READ